박 사 학 위 논 문

Ph.D. Dissertation

정확한 위상 측정이 가능한 저전력 생체임피던스 센서 회로

Low Power Bio-Impedance Sensor IC with Precise Phase Measurement

2021

김 관 태 (金 官 泰 Kim, Kwantae)

한 국 과 학 기 술 원

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위 논문은 한국과학기술원 박사학위논문으로
학위논문 심사위원회의 심사를 통과하였음

2020년 11월 26일

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Low Power Bio-Impedance Sensor IC with Precise Phase Measurement

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Advisor: Hoi-Jun Yoo

A dissertation/thesis submitted to the faculty of
Korea Advanced Institute of Science and Technology in
partial fulfillment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

Daejeon, Korea
November 26, 2020

Approved by

Hoi-Jun Yoo, KAIST
Professor of Electrical Engineering

The study was conducted in accordance with Code of Research Ethics[1)].

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DEE 김관태. 정확한 위상 측정이 가능한 저전력 생체임피던스 센서 회로. 전기및전자공학부. 2021년. 83+ⅳ 쪽. 지도교수: 유회준. (영문 논문)

Kwantae Kim. Low Power Bio-Impedance Sensor IC with Precise Phase Measurement. School of Electrical Engineering. 2021. 83+ⅳ pages. Advisor: Hoi-Jun Yoo. (Text in English)

초 록

흉부 임피던스의 크기 및 위상 측정을 통한 지속적인 체액 상태의 측정은 만성 심부전 환자들의 사망률을 줄이는데 있어 매우 중요하다. 그러나, 체내 이식형 장치에 활용하기 위해 요구되는 엄격한 전력 제약은 생체 임피던스 센서의 설계를 매우 까다롭게 만들고 있다. 본 연구에서는 생체 임피던스 감지 분야를 위한 두 개의 저전압 및 저전력 집적회로가 제안되었으며, 두 집적회로 모두 65 nm CMOS 공정에서 제작되었다.

첫번째 집적회로는 0.5 V의 공급전압에서 10 μW 미만의 전력 소비량을 특징으로 가지며, 공급전압의 10%, 혹은 0°C-70°C의 온도 변동에서도 1° 미만의 위상 오류를 유지한다. 이 집적회로는 4.83 mm^2의 활성 영역을 가지면서 15.28 mΩ/√Hz의 입력 기준 임피던스 잡음 성능을 갖도록 설계되었다. 선형성 성능은 부하 임피던스의 크기가 126 Ω 미만인 조건에서 생체 임피던스의 크기와 위상을 각각 2% 및 0.4° 의 오차 내에서 측정할 수 있음을 보여주므로, 체액 상태 측정에 활용하기 적합하다. 제안된 집적회로는 인체 흉부 임피던스 변동량 및 임피던스 심박동 기록법의 측정을 통해서도 동작성이 검증되었다.

두번째 집적회로는 10 μW 미만의 전력 소비량 및 0.1% 미만의 총 고조파 왜곡 성능을 20 kHz 출력 조건에서 갖추는 정현파 전류 생성기를 특징으로 가진다. 이 집적회로 또한 0.5 V의 공급전압에서 작동하며, 디지털 회로의 임계 값 근처 작동의 초저전력 특성을 활용한다. 제안된 전류 생성기는 2 μA_{pp} 진폭의 정현파 전류를 출력할 때 2 kΩ의 부하 임피던스까지 1% 미만의 구동 오류를 보장하며, 0.059 mm^2의 활성 영역을 가진다.

핵 심 낱 말 생체 임피던스, 만성 심부전, 심박수, 임피던스 심박동 기록법, 이식형 장치, 입력 기준 임피던스 잡음, 좌심실박출시간, 저전압, 위상, 흉부 임피던스 변동량

Abstract

Continuous monitoring of fluid status through bio-impedance (Bio-Z) measurement of thoracic magnitude or phase is critical in reducing the mortality of chronic heart failure (CHF) patients. However, the stringent power constraints of implantable devices force the design of Bio-Z sensors to be highly challenging.

In this dissertation, two low-voltage and low-power ICs are proposed for bio-impedance (Bio-Z) sensing applications, both of which are fabricated in a 65 nm CMOS process.

The first IC features a sub-10-μW power consumption operating from a 0.5 V supply, sustaining a sub-1º of phase error even under 10% of supply and 0ºC–70ºC of temperature variations. It exhibits a 15.28 mΩ/√Hz of

input-referred impedance noise performance, occupying a 4.83 mm^2 of active area. Its linearity performance shows that the magnitude and the phase of Bio-Z can be measured within the error of 2% and 0.4º, respectively, given that the magnitude of load impedance is less than 126 Ω, and thus, it is suitable for fluid status monitoring applications. Experimental measurement on the human chest demonstrates its capabilities of thoracic impedance variance (TIV) and impedance cardiography (ICG) monitoring.

The second IC features a sub-10-μW and a sub-0.1% THD sinusoidal current generator (CG) that is capable of 20 kHz output current driving. This IC also operates from a 0.5 V supply, benefiting from the ultra-low-power nature of near-threshold operation of digital circuit. With a 2 μA_{pp} amplitude of sinusoidal current, it assures <1% of driving error up to the load impedance of 2 kΩ, occupying a 0.059mm^2 of active area.

Keywords Bio-Impedance (Bio-Z), chronic heart failure (CHF), heart rate (HR), impedance cardiography (ICG), implantable device, input referred impedance noise, left-ventricular ejection time (LVET), low supply, phase, thoracic impedance variance (TIV)

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Chapter 1. Introduction

In recent years, bio-impedance (Bio-Z) measurement has been an emerging research area in physiological monitoring applications, such as cardiovascular disease [1]-[3], lung ventilation [4], [5], or breast cancer [6]. Especially with the growing demand for continuous healthcare monitoring in ambulatory chronic heart failure (CHF) patients, the Bio-Z is regarded as an important medical parameter for not only improving survival rates but also reducing hospitalization rates [7]–[10]. This is because common symptoms of the CHF are not recognized by the patients which cause late treatment, leading to severe death rates of the hospitalized CHF patients (10.4% within a month [11] and 40% within a year [10]). Since the Bio-Z tracks conductance of organs by a magnitude ($|Z(j\omega)|$) measurement, preemptive detection of fluid overload is possible and it allows appropriate intervention in proper time. According to [7], it is expected that the impending decompensated heart failure can be detected on average 15 days in advance. Furthermore, phase (φ) measurement of the Bio-Z at a single frequency of several tens of kilohertz reveals the information of water distribution around cell membranes that can also be used for fluid status monitoring of the patients [12]. Therefore, a Bio-Z sensor that is integrated within an implantable device is required in order to conduct long-term fluid status monitoring of the CHF patients by acquisition of ambulatory Bio-Z data, considering its promising clinical potential for preventing hospitalization and early detection of impending decompensated heart failures [7], [10]. One possible implementation method of such device is an implantable cardiac pacemaker system [2], [3].

1.1 Measurement of the Bio-Z

Figure 1 shows the measurement environment of the Bio-Z. When the sinusoidal AC current is injected into the human body through current generator (CG), voltage difference is measured by readout and the Bio-Z can be acquired according to Ohm's law. Typically, one more electrode is used for biasing human body to set the proper DC voltage in order to interface with the sensor IC. Although 5-electrodes are used for the Bio-Z measurement, considering the core part of the measurement are 2-electrodes for current injection and 2-electrodes for voltage monitoring, this measurement setup is called as tetra-polar electrode configuration. An alternative way of the electrode setup includes bi-polar electrode configuration [13], [14], however, the bi-polar

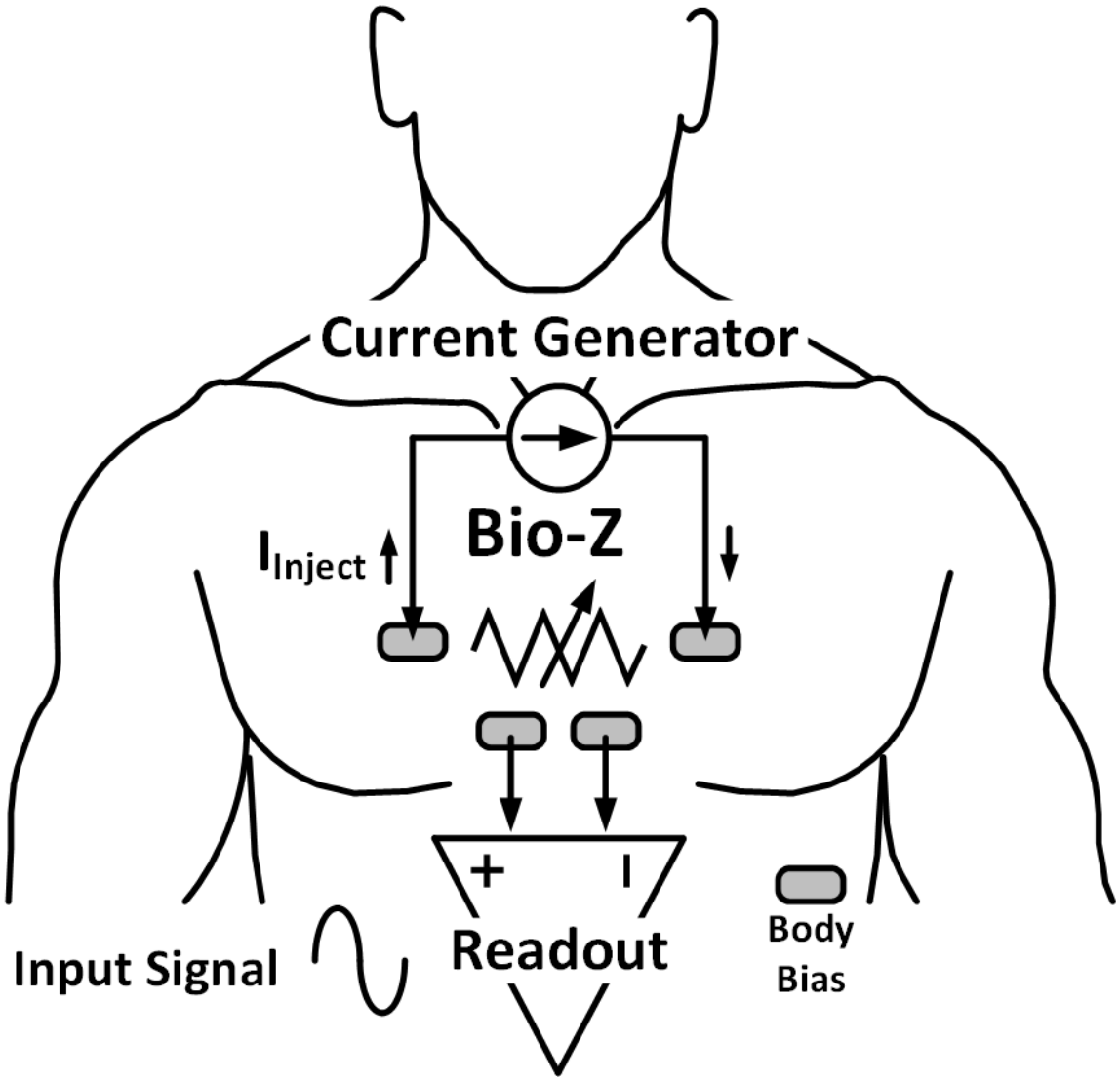

Figure 1. Measurement environment of the Bio-Z.

electrode configuration can not nullify the electrode-related inaccuracies. As such, in contrary to the measurement of the bio-potential signals such as electrocardiogram (ECG) [15] or electroencephalogram (EEG)

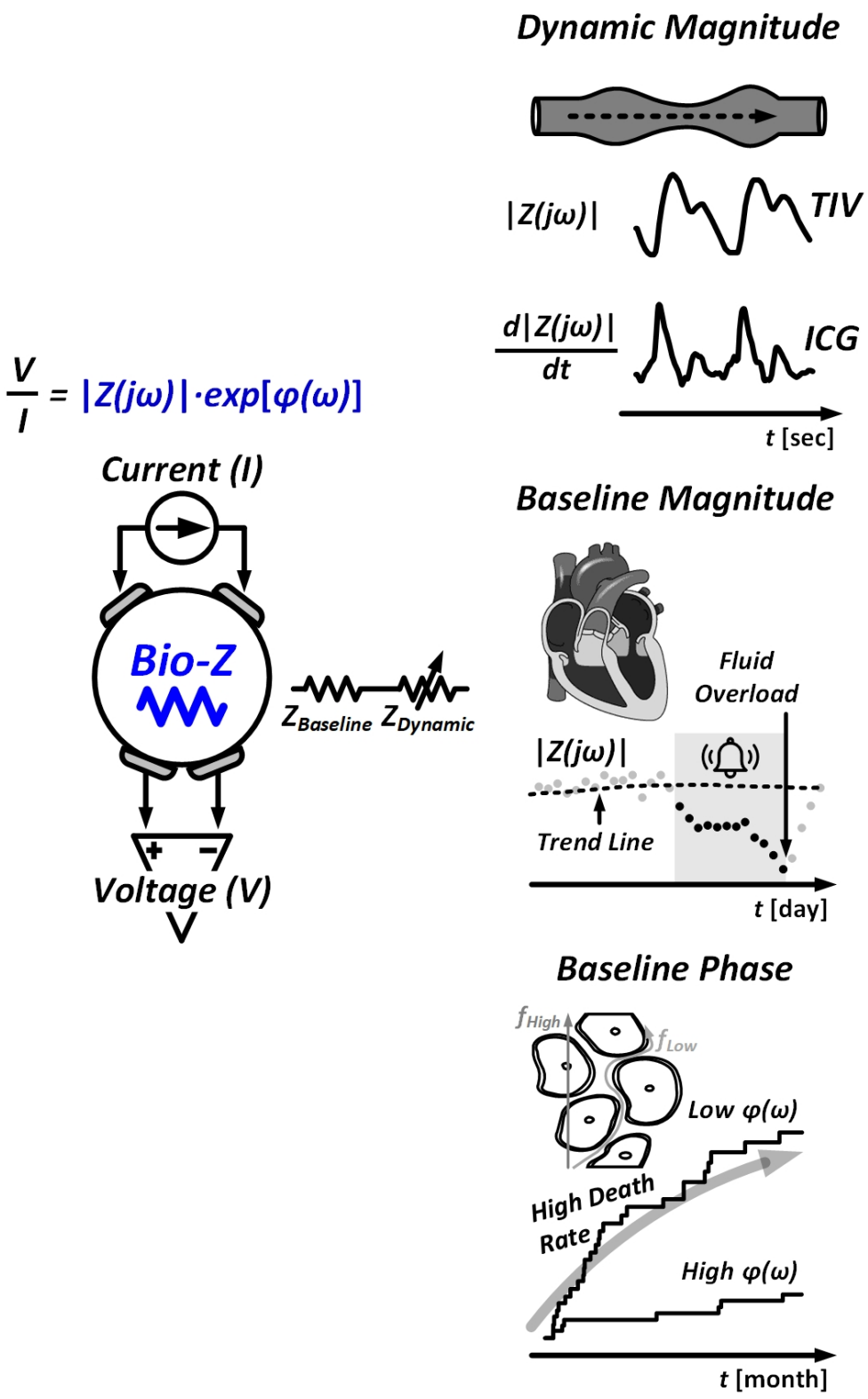

Figure 2. Baseline/dynamic signals of the Bio-Z.

[16], of which activation current is generated by organs inside the human body, the requirement of CG for AC current injection complicates design of the Bio-Z sensor IC.

Figure 2 describes the signals of baseline and dynamic Bio-Z components, also showing their related medical applications. Typically, baseline component has ~100× larger value than its dynamic counterpart, as usual in photoplethysmography (PPG) recordings [17]. The dynamic magnitude represents heartbeat-related blood flow, and therefore its frequency band is usually limited to less than a 10Hz [3] (or 4Hz [13]), which can be measured on human chest (TIV) [1] or human wrist [18], [19] in case the target system is a watch-type wearable healthcare applications. If this dynamic magnitude is 1st-order differentiated in time, impedance cardiography (ICG) is calculated, allowing the estimation of stroke volume or cardiac output [1]. Both of them are useful medical signals for monitoring patient's fluid status. The baseline magnitude and baseline phase of the Bio-Z are also useful signals for preemptive detection of fluid overload and death rate reduction respectively, as discussed in the earlier paragraphs. Especially for the measurement of baseline phase, since the phase response of Bio-Z for the human body ranges within only a few degrees, an accurate (<1º) phase measurement capability is required in the Bio-Z sensors in order to derive a meaningful prognostic medical parameter, considering that the death rate reduction from 30% to 5% even when the Bio-Z phase within the CHF patients differs only a 1.5º [12]. The aforementioned baseline Bio-Z signals are required to be measured in months of long-term duration and thus the Bio-Z readout circuit should be able to capable of DC-coupled measurement. Therefore, two-electrode [13], [14] configuration of the Bio-Z measurement is inadequate approach for the fluid-status monitoring applications because the baseline impedance also includes electrode-tissue impedance (ETI).

1.2 Specifications of the Bio-Z Sensor

1.2.1 Impedance Resolution (Input Referred Impedance Noise)

Impedance resolution refers for the capability of the sensor that how much tiny impedance can be measured. Based on the fact that the Bio-Z is measured by a voltage difference when a certain amount of AC current is injected to the human body, the root-mean-square (RMS) impedance resolution (Z_{RMS}) is defined as [20]

$$Z_{RMS} = \frac{V_{OUT,RMS}}{A_{READOUT} \cdot I_{CG,RMS}} \tag{1}$$

where $V_{OUT,RMS}$ is the RMS voltage noise measured at the output of the readout, accounting for the noise contribution from the CG [13], $A_{READOUT}$ is the gain of readout circuit, $I_{CG,RMS}$ is the RMS amplitude of the injection current from the CG. Note that the term of $V_{OUT,RMS}$ is different from the classical output referred noise (ORN), which only includes the noise contribution of the readout circuit alone.

In general, the Bio-Z sensor should have less than a 0.1 Ω_{RMS} resolution, which corresponds to a 31 mΩ/√Hz input-referred impedance noise in a 10 Hz bandwidth (BW) or a 50 mΩ/√Hz in a 4 Hz BW, in order to detect small impedance variations of dynamic magnitude (e.g. blood flow in vessels). As shown in Equation (1),

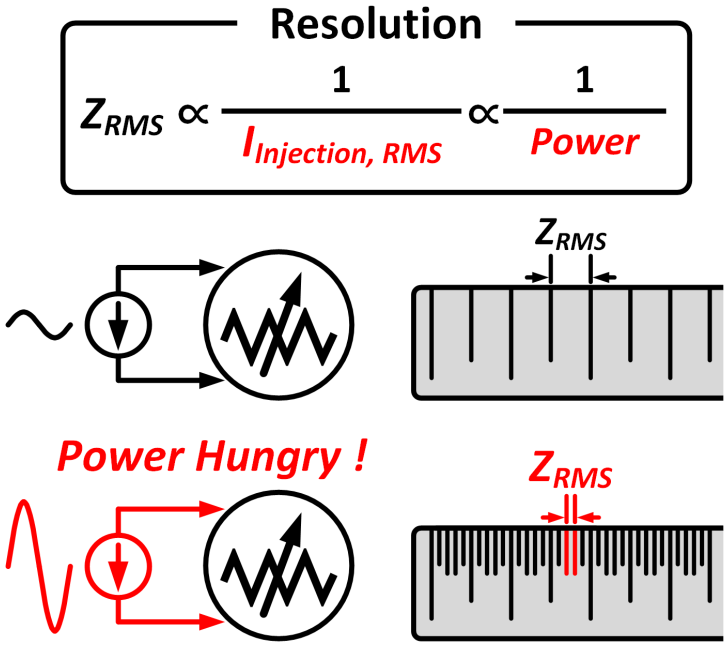

Figure 3. Impedance resolution and the power overhead.

the impedance resolution can be enhanced by injecting a large amount of current amplitude or reducing the noise amount appearing at the output of readout. However, these approaches have direct relationship to the large amount of power consumption. For example, as illustrated in Figure 3, since the resolution of the Bio-Z sensor is inversely proportional to the injected amount of current amplitude, it poses difficulty to achieve a high-resolution and a low-power operation at the same time, considering the stringent power budget of an implantable devices, for example, cardiac pacemaker system that should ensure >10 years of lifetime and a sub-10 μW of power consumption [2], [3]. Even if the designer ignore power budget of the Bio-Z sensor, to meet the international safety regulations, a sinusoidal current ranging from 10kHz to 100kHz can not be injected into the human body above the amplitude of 1 mA_{RMS} [21]. Therefore, a dedicated circuit design techniques are required for the high-performance Bio-Z sensor system, including the design of low-noise readout and low-power sinusoidal signal generator.

1.2.2 Impedance Sensitivity

In a classical definition of the sensitivity, it refers to the amount of output variation given that a certain amount of input changes. For example, the sensitivity of Q-factor in filter circuits to the pre-defined parameter of n is derived as below.

$$S_Q^n = \frac{\partial Q}{\partial n} / \frac{Q}{n} \tag{2}$$

In the case of Bio-Z sensors, sensitivity refers to the measured output voltage amount with a unit change of impedance, and its dimension has [V/Ω] as described in [1].

$$S_V^\Omega = \frac{\partial V}{\partial \Omega} / \frac{V}{\Omega} \tag{3}$$

Sensitivity is important specification especially in the applications demanding for the high-contrast data at the output of voltage readout, even if the tiny changes are detected on the input impedance, such as EIT. Although some papers [5], [22]-[24] used different definitions of sensitivity (referring to the quantized input-referred noise instead of using resolution), in this dissertation, sensitivity will not be used for referring to the noise-related specification.

1.2.3 Total Harmonic Distortion of the Current Generator

Since the measurement procedure of the Bio-Z starts from the injecting a clean sinusoidal AC current, it obvisouly necessitates a low-distortion sinewave on the current signal. For example, less than 1% of total harmonic distortion (THD) after the demodulation was used in the implantable pacemaker system [2], [3], while even much tighter THD of less than 0.5% at the output of current waveform was desired for the EIT applications [5], [6]. This is because the sinewave-modulated Bio-Z voltage signal is typically demodulated to the baseband using chopper, which is square-wave signal, for a low-power and simplest implementation. In this case, any of odd harmonic components existing in the sinewave of injection current will be demodulated to the baseband through chopping, because chopping signal as a square-wave, also contains odd harmonic components. Further discussions of modulation and demodulation of the Bio-Z during the measured will be provided in Chapter 2.

Chapter 2. Review of the Bio-Z Modulation Techniques

It is well known that the Bio-Z measurement based on a square-wave modulation is highly erroneous for measuring both of the magnitude ($|Z(j\omega)|$) and the phase (φ) [2], [25], [26]. Since the CG acts as a modulator of the Bio-Z with a given frequency, odd-harmonic components of the square-wave spectrum unavoidably collect the incorrect Bio-Z data. When the widely used demodulation technique of chopping is utilized for simplicity and a low-power design, which is also a square wave, it leads to a severely contaminated baseband Bio-Z signal. This is due to the aliased odd-harmonic components of the square wave [3]. Assuming the conventional chopper-based I/Q demodulation scheme is adopted, equations of quadrature square-wave clocks are given by as below.

$$V_{ICLK}(t) = \frac{4}{\pi} \times \sum_{n=odd}^{\infty} \frac{\sin(n\omega_0 t)}{n} \tag{4}$$

$$V_{QCLK}(t) = \frac{4}{\pi} \times \sum_{n=odd}^{\infty} \frac{\cos(n\omega_0 t)}{n} \tag{5}$$

In this Chapter, we will analyze and discuss the I/Q demodulated readout voltage equations for each type of three modulation cases (pure-sine, square-wave, pseudo-sine). Using the derived equations, the achievable phase accuracy will be simulated with a known RC model of the Bio-Z [26].

2.1 Pure-Sine Modulation

If a pure-sinusoidal current I with a known amplitude and frequency ω_0 is injected, a voltage difference $V_{mod,S}(t)$ is generated with a phase shift φ_0 arising from the capacitive effects of Bio-Z cell membrane. This can be expressed as

$$V_{mod,S}(t) = I \times |Z(\omega_0)| \sin(\omega_0 t + \varphi_0) \tag{6}$$

where $|Z(j\omega)|$ is a magnitude of the Bio-Z data at ω_0. Assuming a low pass filter (LPF) is implemented following the demodulation path such that high frequency components of demodulated signals can be largely attenuated, resulting the I/Q demodulated readout voltages can be expressed by

$$V_{IOUT,S}(t) = V_{ICLK}(t) \times V_{mod,S}(t) \approx \frac{2}{\pi} I \times Z(\omega_0) \cos(\varphi_0) \tag{7}$$

$$V_{QOUT,S}(t) = V_{QCLK}(t) \times V_{mod,S}(t) \approx \frac{2}{\pi} I \times Z(\omega_0) \sin(\varphi_0) \tag{8}$$

The achievable Bio-Z phase data using (7) and (8) results in

$$\tan^{-1}\left(\frac{V_{QOUT,S}(t)}{V_{IOUT,S}(t)}\right) = \varphi_S = \varphi_0 \tag{9}$$

Equation (9) shows that the pure-sine modulation scheme measures the Bio-Z phase without any errors. However, designing a low harmonic pure-sine oscillator comes with a huge amount of power consumption ranging in 100 μW to several milliwatt scale [1], [4], [6], which is not suitable for continuous blood-status monitoring applications such as implantable pacemaker system.

Graphical illustration of pure-sine modulation is shown in Figure 4, also showing the used RC model of the Bio-Z [26]. A 10 kHz is arbitrarily chosen by considering typical range of modulation frequency for the Bio-Z measurement [1], [3], [6], [23], [27], [29], [30]. Each circle represents where the Bio-Z is modulated. As expected in Equation (6), there is only one circle for the pure-sine modulation case for both of magnitude and phase plot at 10 kHz since the purely sinusoidal wave is composed of single tone in spectrum.

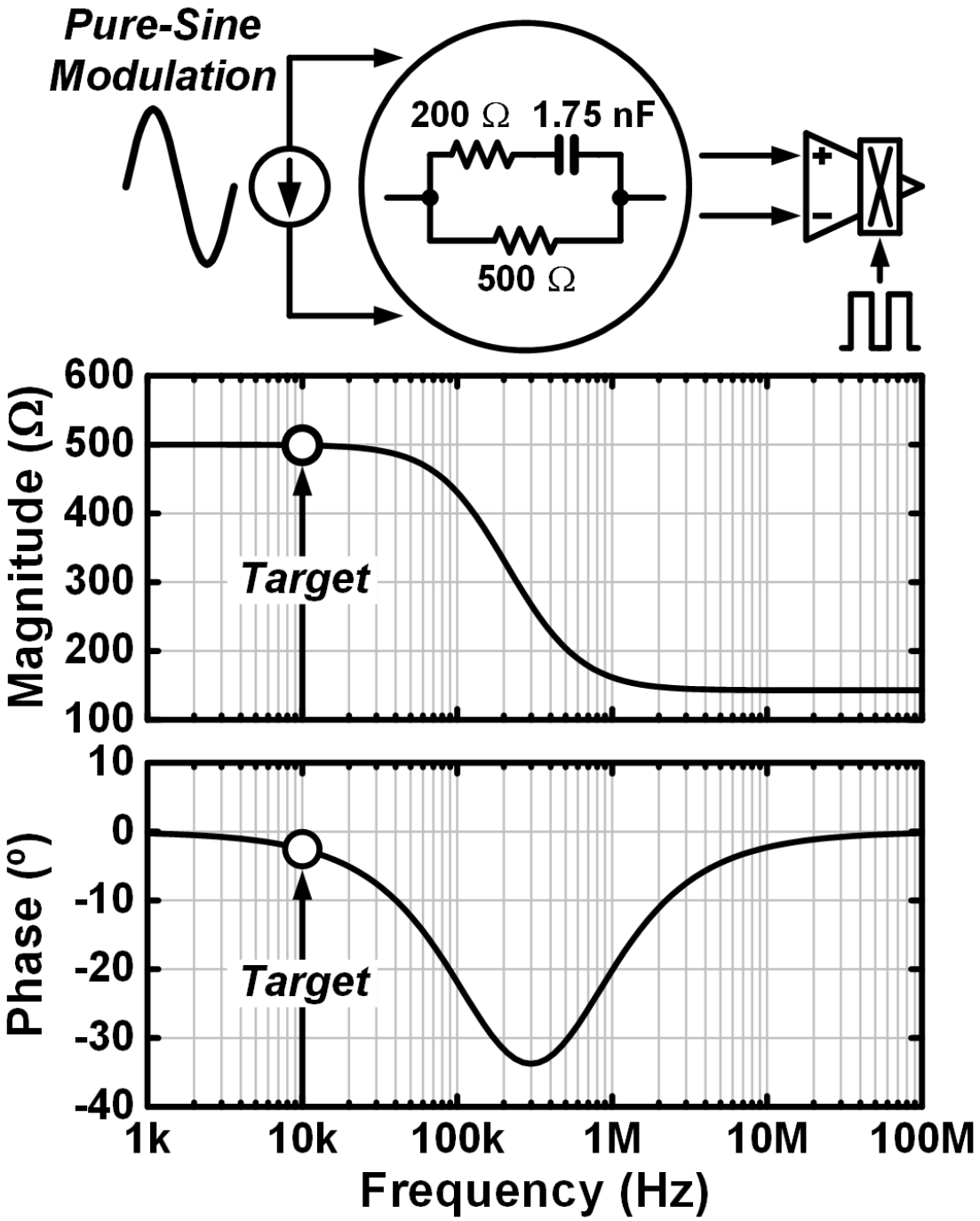

Figure 4. Conceptual diagram of the modulation scheme based on pure-sine waveform.

2.2 Square-Wave Modulation

The equation of the square-wave modulated voltage signal can be expressed as a sum of all odd harmonics which is similar to (4), but including the magnitude and the phase data of Bio-Z as given by

$$V_{mod,SQ}(t) = \frac{4}{\pi} \times \left[|Z(\omega_0)| \sin(\omega_0 t + \varphi_0) + \frac{|Z(3\omega_0)| \sin(3\omega_0 t + \varphi_3)}{3} + \frac{|Z(5\omega_0)| \sin(5\omega_0 t + \varphi_5)}{5} + \frac{|Z(7\omega_0)| \sin(7\omega_0 t + \varphi_7)}{7} + \frac{|Z(11\omega_0)| \sin(11\omega_0 t + \varphi_{11})}{11} + \cdots \right] \tag{10}$$

where φ_n denotes the phase data of Bio-Z at $n\omega_0$. Also assuming the LPF is implemented that is sufficient to ignore higher orders of harmonics of demodulated signals, resulting I/Q demodulated readout voltages can be derived as shown in (11) and (12).

$$V_{IOUT,SQ}(t) = \left(\frac{4}{\pi}\right)^2 \frac{I}{2} \times \left[|Z(\omega_0)| \cos(\varphi_0) + \frac{|Z(3\omega_0)| \cos(\varphi_3)}{3^2} + \frac{|Z(5\omega_0)| \cos(\varphi_5)}{5^2} + \cdots \right] \tag{11}$$

$$V_{QOUT,SQ}(t) = \left(\frac{4}{\pi}\right)^2 \frac{I}{2} \times \left[|Z(\omega_0)| \sin(\varphi_0) + \frac{|Z(3\omega_0)| \sin(\varphi_3)}{3^2} + \frac{|Z(5\omega_0)| \sin(\varphi_5)}{5^2} + \cdots \right] \tag{12}$$

Since the derived equations of I/Q demodulated readout voltages include several odd harmonic terms, we can expect that the resulting Bio-Z phase data would be erroneous (Figure 5). Equating (11) and (12) with the arctangent function gives the Bio-Z phase data using the square-wave modulation scheme, expressed as below.

$$\tan^{-1}\left(\frac{V_{QOUT,SQ}(t)}{V_{IOUT,SQ}(t)}\right) = \varphi_{SQ} \tag{13}$$

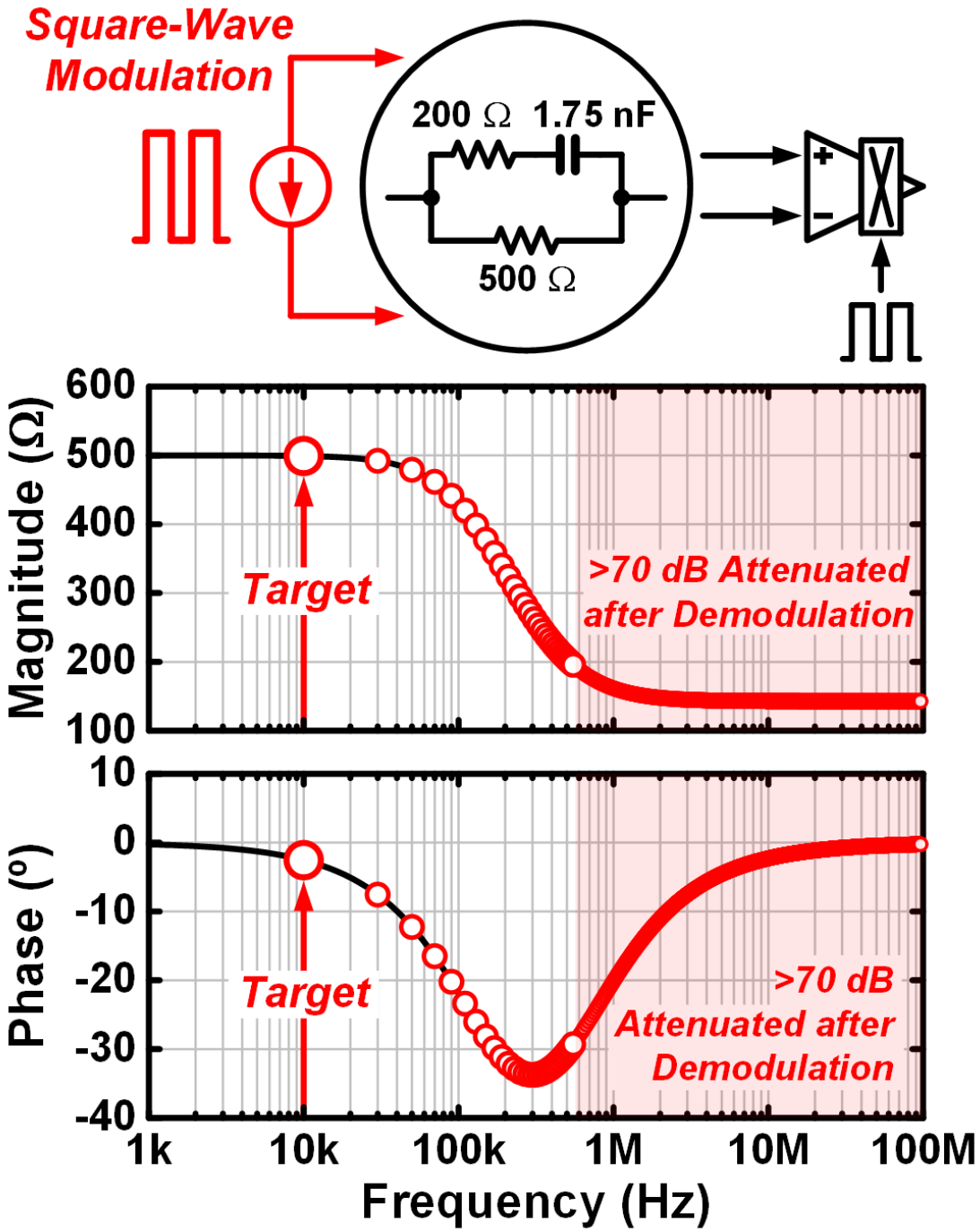

Figure 5. Conceptual diagram of the modulation scheme based on squre-wave waveform.

2.3 Pseudo-Sine Modulation

As demonstrated in [2], [3], [27], a pseudo-sine modulation scheme for the Bio-Z measurement provides a good power and accuracy tradeoff. Also known as direct digital synthesis (DDS) technique, it uses a look-up table (LUT) combined with a digital to analog converter (DAC) to shape a low-distortion sinusoidal waveform. Given that the ratio of clock to output frequency is 64, the modulated Bio-Z signal can be expressed as below [3], [28].

$$V_{mod,PS}(t) = I \times \left[|Z(\omega_0)| \sin(\omega_0 t + \varphi_0) + \frac{|Z(63\omega_0)| \sin(63\omega_0 t + \varphi_{63})}{63} + \frac{|Z(65\omega_0)| \sin(65\omega_0 t + \varphi_{65})}{65} + \frac{|Z(127\omega_0)| \sin(127\omega_0 t + \varphi_{127})}{127} + \frac{|Z(129\omega_0)| \sin(129\omega_0 t + \varphi_{129})}{129} + \cdots \right] \quad (14)$$

Assuming the same conditions of a LPF is designed as described above, resulting I/Q demodulated readout voltages of pseudo-sine modulation scheme are given by below.

$$V_{IOUT,PS}(t) = \frac{2}{\pi} I \times \left[|Z(\omega_0)| \cos(\varphi_0) + \frac{|Z(63\omega_0)| \cos(\varphi_{63})}{63^2} + \frac{|Z(65\omega_0)| \cos(\varphi_{65})}{65^2} + \cdots \right] \quad (15)$$

$$V_{QOUT,PS}(t) = \frac{2}{\pi} I \times \left[|Z(\omega_0)| \sin(\varphi_0) + \frac{|Z(63\omega_0)| \sin(\varphi_{63})}{63^2} + \frac{|Z(65\omega_0)| \sin(\varphi_{65})}{65^2} + \cdots \right] \quad (16)$$

Comparing with (11), (12), we can see that the odd harmonic components of demodulated readout voltages are highly attenuated (>632 = 71.97 dB) using the pseudo-sine modulation scheme (Figure 6). From (15) and (16), the Bio-Z phase data based on the pseudo-sine modulation scheme is expressed as below.

$$\tan^{-1}\left(\frac{V_{QOUT,PS}(t)}{V_{IOUT,PS}(t)}\right) = \varphi_{PS} \quad (17)$$

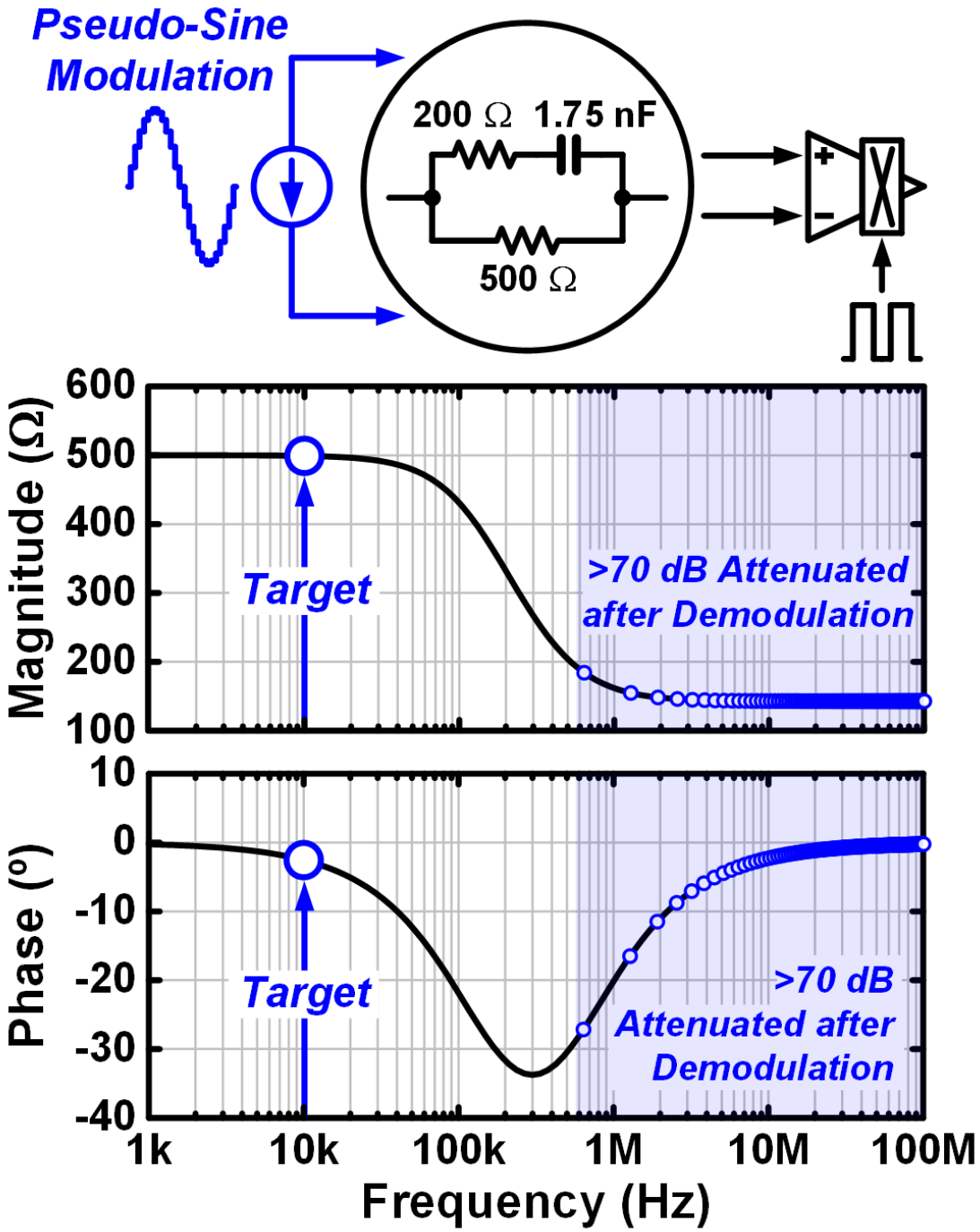

Figure 6. Conceptual diagram of the modulation scheme based on pseudo-sine waveform.

2.4 Simultaion Results with RC Model

To assess and compare the theoretical results discussed so far, numerical simulation is also conducted in order to verify the measurement accuracy of Bio-Z phase for both of the square-wave and pseudo-sine modulation schemes, using MATLAB. Figure 7 shows a plot of the theoretically achievable Bio-Z phase accuracy for each of modulation schemes, based on (13) and (17). Up to 960th harmonics are included. It is clearly seen that square-wave modulation scheme introduces intolerable phase error up to 2.99º, which is not acceptable for making any diagnostic decisions [26]. However, based on the pseudo-sine modulation, phase error is reduced down to negligible value that is less than 0.02º, indicating that it is optimal solution for the long-term fluid-status montiroing applications.

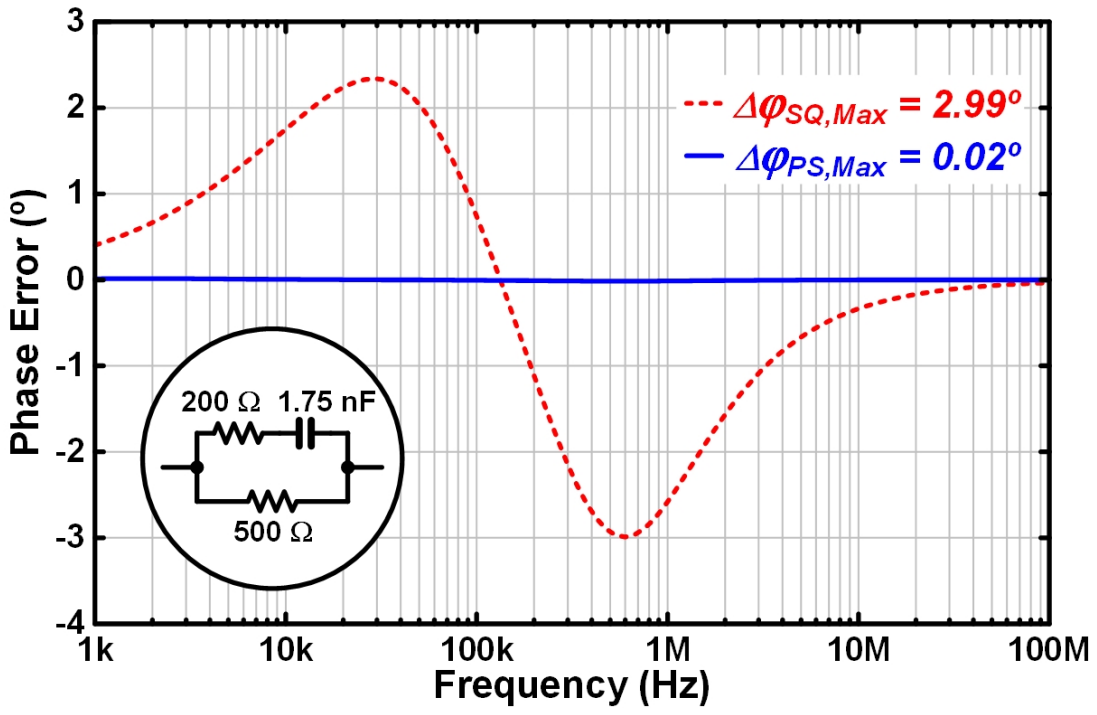

Figure 7. Simulation results of phase error based on the square-wave and pseudo-sine modulation.

Chapter 3. Low-Phase-Error Bio-Z Sensor IC

To meet the design requirements of the implantable fluid status monitoring for the CHF patients as discussed in eariler Chapters, we present a Bio-Z sensor IC [29], [30] that utilizes the following.

1) Supply scaling of the entire sensor front end down to 0.5 V that is the lowest value among the Bio-Z sensors reported ever to achieve low power and high resolution. We propose a dedicated biasing scheme in order to achieve the low-supply operation, including common-mode feedback (CMFB) in the transconductance (TC) stage of the instrumentation amplifier (IA) and temperature-compensated dc biasing scheme of the input transistors.
2) 64× sampled pseudo-sine waveform for the injection current to reduce phase error.
3) A lead-compensated TC stage for the 5.85× improved BW performance in readout leading to a low phase error.
4) A low-dropout regulator (LDO)-based V–I converter with the residual current rejection so that low-power operation is possible.

The overall architecture of the proposed Bio-Z sensor IC is shown in Figure 8. The tetra-polar electrode configuration is adopted to nullify the electrode-related inaccuracies for the Bio-Z measurement

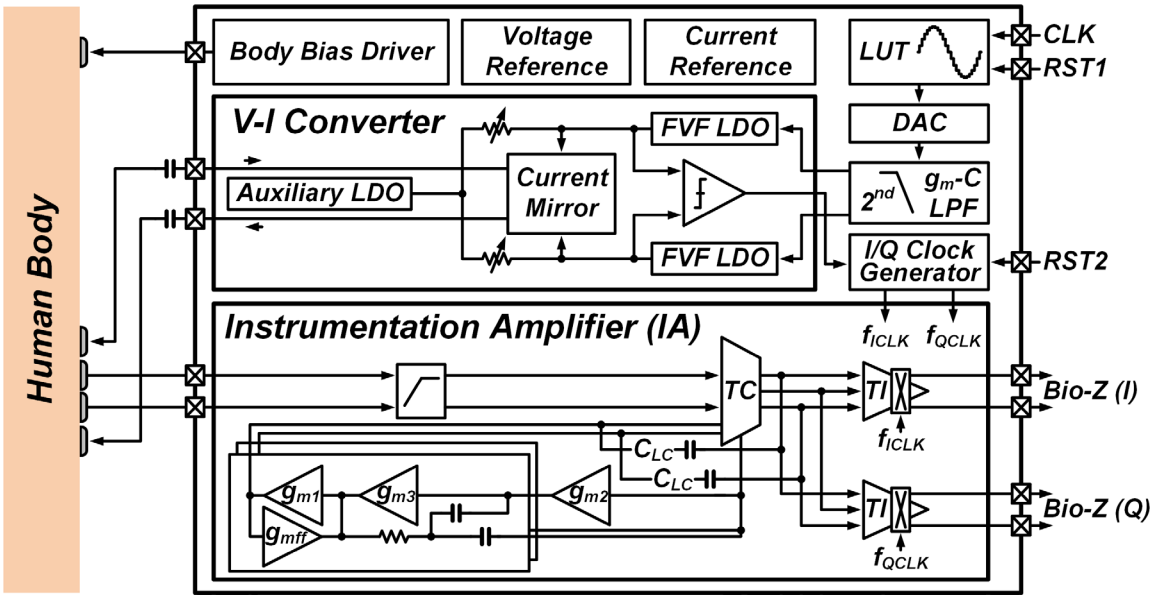

Figure 8. Overall architecture of the proposed Bio-Z sensor IC.

instead of bi-polar electrode configuration [13], [14]. There are five main building blocks within the IC: 1) an IA for low-noise and low-phase shift Bio-Z readout including passive high-pass filter (HPF) for AC-coupling purpose; 2) an LDO-based voltage-to-current (V–I) converter for low-power current injection; 3) an LUT, a 6 bit capacitive voltage DAC, and a second-order g_m-C LPF [31] for low harmonic sinusoidal synthesis; 4) an I/Q clock generator to create the quadrature demodulation clocks that are phase-aligned to the injection current; and 5) bias circuits comprising a voltage and a current references, and a body bias driver in order to set a DC bias voltage on the human body. Off-chip AC-coupling capacitors (C_{AC}) are connected in a series configuration on the injection current path, considering safety of patients [21] and electrode degradation issues [32].

Figure 9 shows the dominant phase error contributors for the Bio-Z measurement. When a 1.28-MHz external clock is driven to the LUT to synthesize pseudo-sine waveform, a 20-kHz sinusoidal current is injected

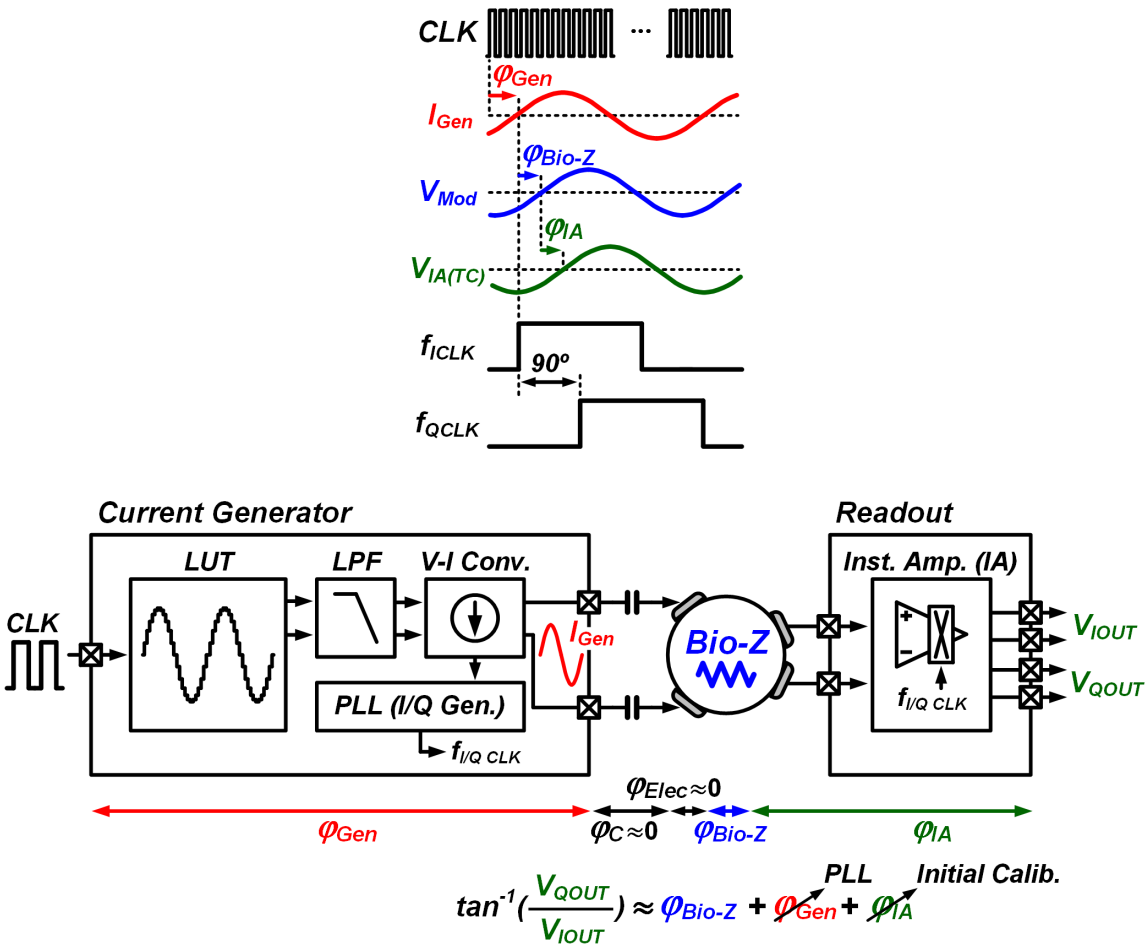

Figure 9. Dominant contributors of phase error for the Bio-Z measurement.

to the human body by a V–I conversion after it is low-pass filtered. Since there is a finite phase shift within the LPF and the V–I converter, the current generator introduces the phase error of φ_{Gen}. Besides, C_{AC} and the capacitive components of the electrodes also contribute to the phase error, denoted as φ_{C} and φ_{Elec}. When the injected sinusoidal current of I_{Gen} flows through the human body, it is multiplied by the Bio-Z and the modulated Bio-Z voltage signal includes phase data ($\varphi_{Bio\text{-}Z}$). Last but not least, a phase shift due to limited BW of readout circuit introduces another phase error of φ_{IA}. Phase shift of voltage electrodes interfacing with the IA is negligible, given that the input impedance of the IA is sufficiently large. Thus, the measured phase data using the proposed Bio-Z sensor are as below.

$$\tan^{-1}\left(\frac{V_{QOUT}}{V_{IOUT}}\right) = \varphi_{Gen} + \varphi_{C} + \varphi_{Elec} + \varphi_{Bio-Z} + \varphi_{IA} \tag{18}$$

φ_{C} can be reduced down to a negligible value less than 0.1º using a large valued off-chip capacitor for C_{AC} (1 μF). Moreover, φ_{Elec} is also negligible when a sufficiently high frequency of the injection current is utilized. For example, a 10 kHz modulation frequency with implantable electrodes that are used with the pacemakers (43 kΩ||400 μF and 43 kΩ||2 mF [33]) generates a phase error of only 0.05mº and 0.01mº. Note that we can also reduce the phase error down to 0.091º with dry-contact electrodes (1 MΩ||10 nF [34]) if wearable device is utilized.

In this Bio-Z sensor IC, a bang-bang digital phase-locked loop (PLL)-based I/Q clock generator and a wide-BW IA design based on a lead-compensated TC stage are proposed to cope with φ_{Gen} and φ_{IA}, respectively. As shown in Figure 9, by aligning the rising edge of f_{ICLK} to the zero-crossing point of I_{Gen} using the continuous-time comparator and the PLL, φ_{Gen} can be eliminated. In prior works, φ_{Gen} had not been discussed [5], [35], [36] or a huge power dissipation was required to compensate for the phase shift of current generator itself. For instance, [37] used two parallel V–I converters to compensate for the phase shift. However, it leads to a significant power waste because the V–I converter is one of the most powerconsuming blocks within the Bio-Z sensor IC [20]. Since the PLL-based φ_{Gen} compensation method generates the I/Q demodulation clocks according to the zero-crossing point of I_{Gen}, it obviates the need for compensating the phase shift of the V–I converter. Thus, the proposed approach not only minimizes φ_{Gen} but also leads to a low-power operation of the

Bio-Z sensor. Furthermore, a wide-BW IA design allows the changes of φ_{IA} that can be minimized down to a sub-1º over the supply and the temperature variations. Therefore, phase error contribution of φ_{IA} will be removed over the process–voltage–temperature (PVT) variations after it is calibrated during an initial operation of the Bio-Z sensor. As a result, the proposed Bio-Z sensor IC can solely measure the phase data of $\varphi_{Bio\text{-}Z}$.

This Chapter is organized as as follows. Chapter 3.1 and Chapter 3.2 introduces the implementation details of the proposed Bio-Z sensor IC. Chapter 3.3 shows the chip measurement results and performance summary, including experimental tests on the human body.

3.1 Design of the 0.5 V Instrumentation Amplifier

The IA of the Bio-Z readout provides a precise gain of voltage amplification with a low-noise performance. Besides, a wide-BW performance is essential for an accurate phase measurement of the Bio-Z to minimize the phase shift of the IA itself. Figure 4 shows a simulated phase shift (φ_{IA}) of the widely used current-feedback IA for the Bio-Z sensors [5]. Although φ_{IA} can be canceled out once by an initial calibration, a large amount of phase error ($\Delta\varphi_{IA}$) arising from the supply and the temperature variations cannot be fully eliminated. In order to make $\Delta\varphi_{IA}$ less than a 1º, a 10× higher BW than the modulation frequency is required. Unfortunately, achieving both a low-noise and a wide-BW performance while consuming an ultra-low power is a very challenging goal because both of them generally necessitate high power consumption.

Several prior works suggested the methods to mitigate readout BW requirements. A calibration method always before the Bio-Z measurement can remove the phase error of the IA once [3], but it can not measure both the Bio-Z baseline phase and dynamic magnitude (e.g. TIV) continuously. A pre-demodulation scheme [13], [38], [22], [23], [36] can transfer modulation frequency of the Bio-Z signal to an intermediate frequency band where it introduces sufficiently negligible phase shift (e.g., <0.1×BW). However, the conversion gain of the sine-to-square-wave demodulation is 2/π, which leads to a degraded SNR by 2/π times. Therefore, pre-demodulation is a power-inefficient technique since it requires additional demodulation step before the IA, leading to a 2.47× increased power budget of the IA to uphold the same noise performance.

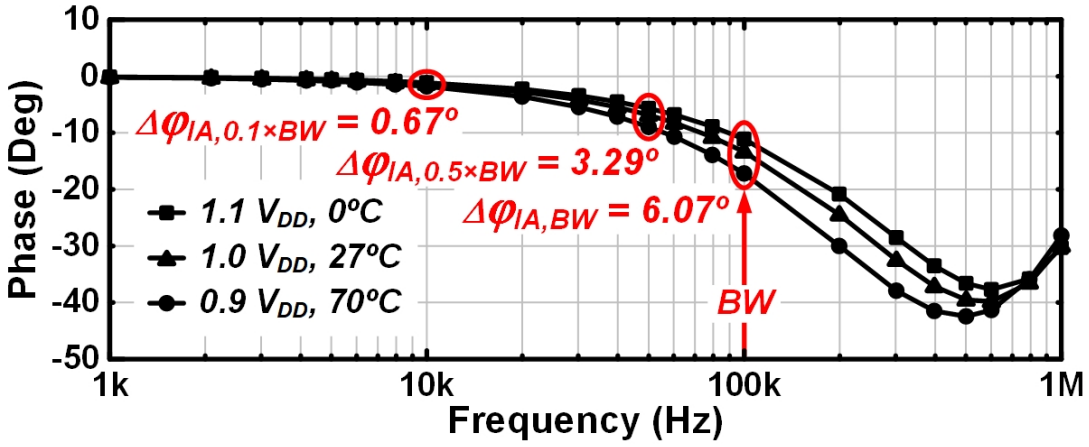

Figure 10. Simulated supply and temperature sensitivity of phase shift for the current-feedback IA.

We propose a current-feedback IA that operates at a 0.5 V supply and it consumes only a 3.95 μW while achieving not only a low-noise performance of 45 nV/√Hz but also a wide BW of 408 kHz. The 0.5 V supply voltage is the lowest operating condition of the Bio-Z sensor ICs ever reported. The key specifications of the proposed IA are the result of optimizations by multiple circuit-level features.

First, a PVT-robust 0.5 V supply operation is realized using dedicated circuit components for stable dc biasing of the proposed IA, utilizing a CMFB loop and a temperature-compensated voltage reference. To the best of our knowledge, the proposed IA is the only work among the various current-feedback IA designs that can ensure stable DC operating conditions, including all of gate, source, and drain nodes of the input transistors.

Second, the pre-demodulation scheme is avoided, which leads to increased power consumption;

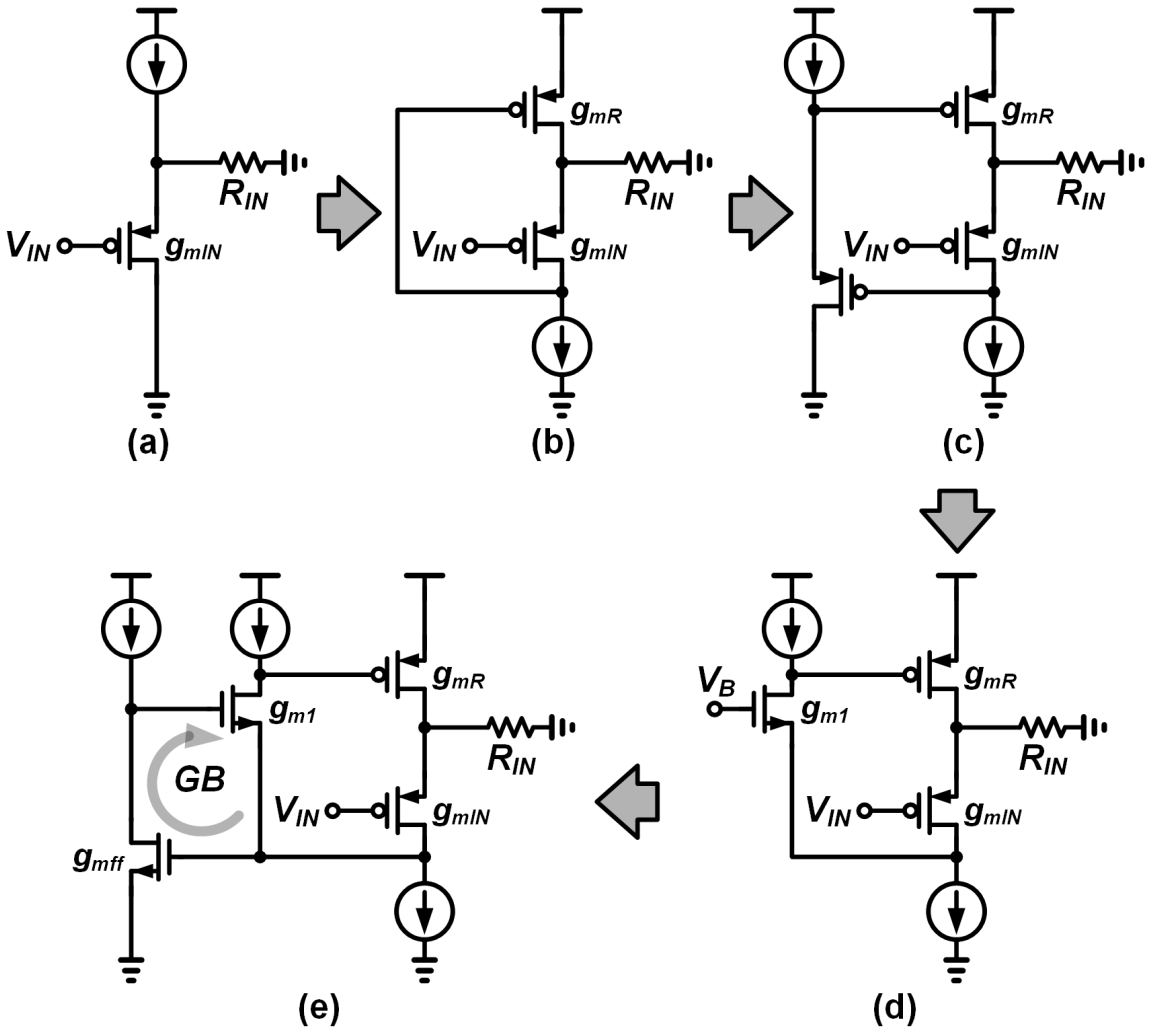

Figure 11. Circuit schematics of (a) basic source follower, (b) FVF, (c) FVF with a source-follower-based level shifter, (d) FVF with a common-gate amplifier, and (e) FVF with a common-gate amplifier and a GB loop.

instead, we propose the lead-compensated TC stage to enhance the BW of the IA that leads to a 5.85× improvement. It is worth mentioning that a low-noise performance of the current-feedback IA typically results in a degraded BW with a given power budget, due to a low-valued input resistor. In the most of prior works, this issue was typically devolved into the simple pre-demodulation technique [13], [38], [22], [23], [36] or not discussed at all [5], [27], [39], [40], leading to the degraded BW. To the best of our knowledge, this article is the first among the Bio-Z sensors that point out the noise–BW tradeoff of the conventional current-feedback IA topology in a limited power budget, providing loop response analysis of the main bottleneck for the BW improvement and also suggests a solution to ensure a wide BW and a low-noise performance through the proposed lead-compensated TC stage.

3.1.1 Transconductance Stage

Figure 11 describes the several flipped voltage follower (FVF) circuit topologies used not only in the TC stage of the current-feedback IA but also in the LDO regulator designs. The main purpose of the FVF usage is an improvement of the input signal buffering capability to the input resistor (R_{IN}), by a negative-feedback loop formed around the input transistor (g_{mIN}) [41], in Figure 11(b). In [39], as shown in Figure 11(c), a source-follower-based level shifter was used to lower the DC operating point of drain node of the input transistor and it ensures its saturation when the incoming common-mode (CM) signal is low. However, instead of using the level shifter, when we configure the FVF circuit with a gain stage, e.g., a common-gate amplifier (g_{m1}) as shown in Figure 11(d), not only the biasing capability of the input transistor using VB but also an improved loop gain can be achieved [42]. Furthermore, if this common-gate amplifier is utilized with a gain-boosting (GB) loop, even more loop gain enhancement can be expected [5]. As shown in Figure 11(e), gate biasing of the common-gate amplifier can be controlled by a common-source amplifier (g_{mff}) and a current source. In addition, drain node biasing of the input transistor can be controlled by V_{GS} of the common-source amplifier. To summarize, various topologies of the FVF circuits are focused on the two design points: 1) obtaining sufficient headroom for the operation of input transistors and 2) enhancing loop gain of FVF itself for the buffering capability of the input transistors.

Although an another circuit topology which is called as super source follow (SSF) was used for the design of the current-feedback IA in [43] as shown in Figure 12, it has severe drawback for the perspective of linear input range and input referred noise performance. The current mirrors depicted in Figure 12 are fundamental principle of the current-feedback IA which will be discussed with Figure 13 in the later paragraphs. Since linear input range of the SSF and the FVF in Figure 12 are defiend as below,

$$Input\ Range = \pm\left(I_{gmR} \times R_{IN}\right) \tag{19}$$

splitted-current branch structure of the SSF has a trade-off between input range and input referred noise performance considering that the noise performance is mainly determined by the input transistor (g_{mIN}) for both of architectures. Note that the current flowing amount of level shifter in FVF is not a dominant factor for noise performance, and thus it can be optimized as a negligible value for example 36× smaller as in [39].

Figure 13 shows the circuit schematic of the proposed current-feedback IA that is composed of two stages: a TC stage and a transimpedance (TI) stage. The principle of the current-feedback IA operation is based on an FVF feedback loop of the TC stage as shown in Figure 11(e), to buffer the input voltage signals to R_{IN}. Generated current signal from a voltage difference across R_{IN} is mirrored to the TI stage. Thus, the gain of the current-feedback IA can be designed as a known value based on R_{IN}, R_{OUT}, and the current mirroring ratio.

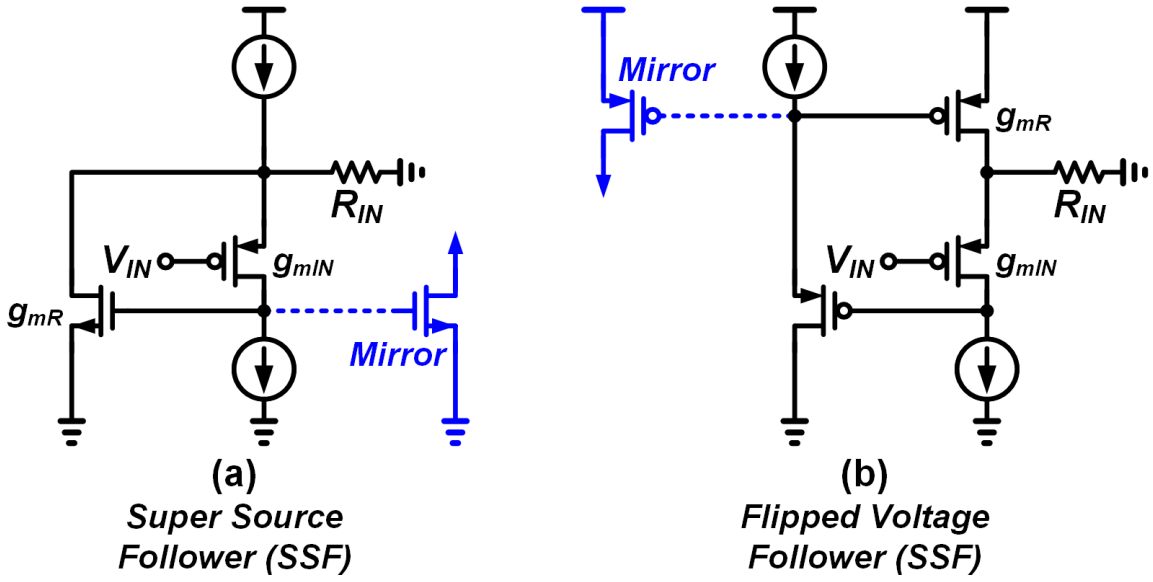

Figure 12. Circuit schematics of (a) super source follower, (b) FVF with a source-follower-based level shifter.

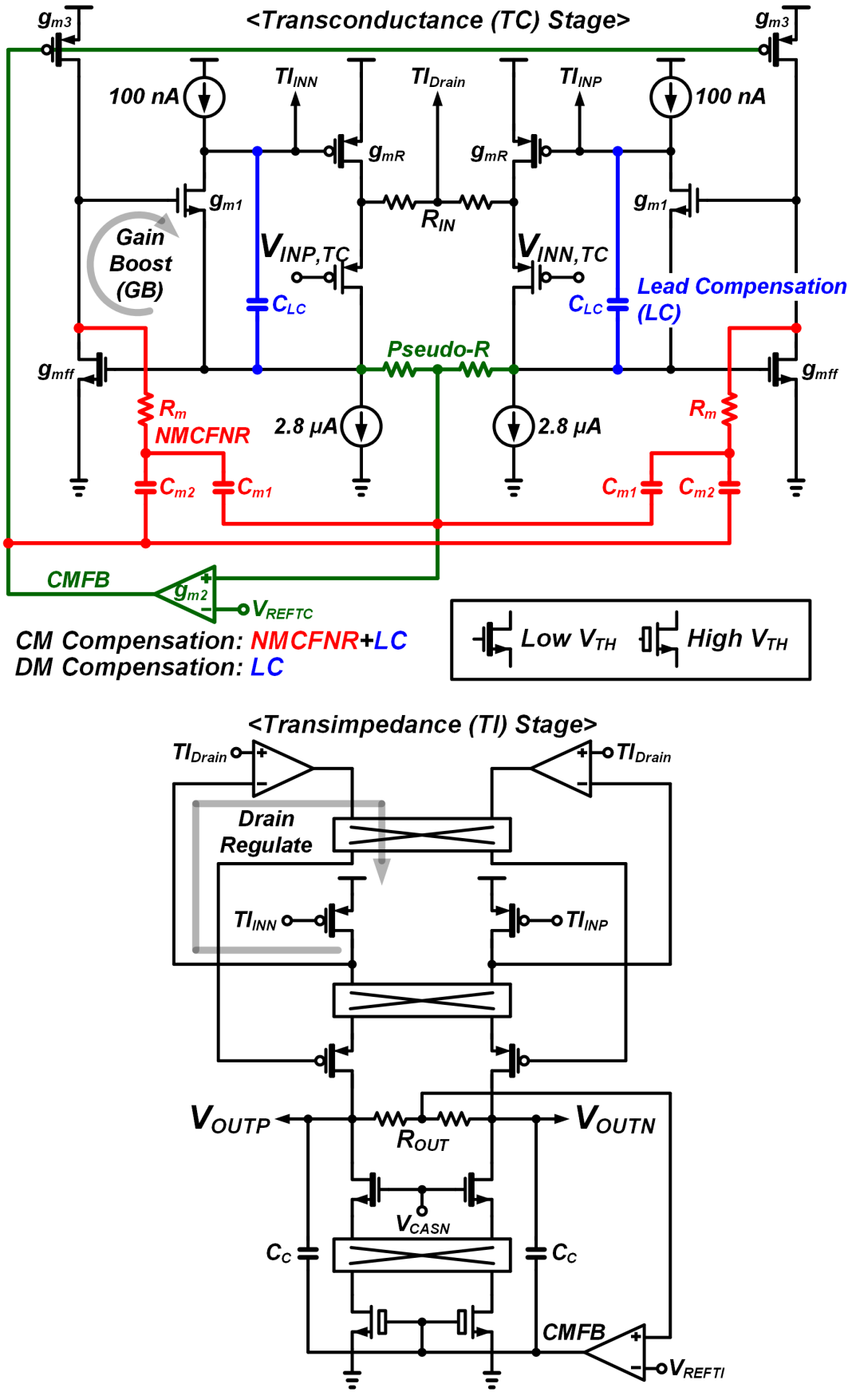

Figure 13. 0.5 V supply current-feedback IA.

For a low-supply operation, a CMFB loop is adopted to stabilize the drain node of the input transistor over PVT corners by a known value (V_{REFTC}). It has an advantage in terms of headroom compared with the

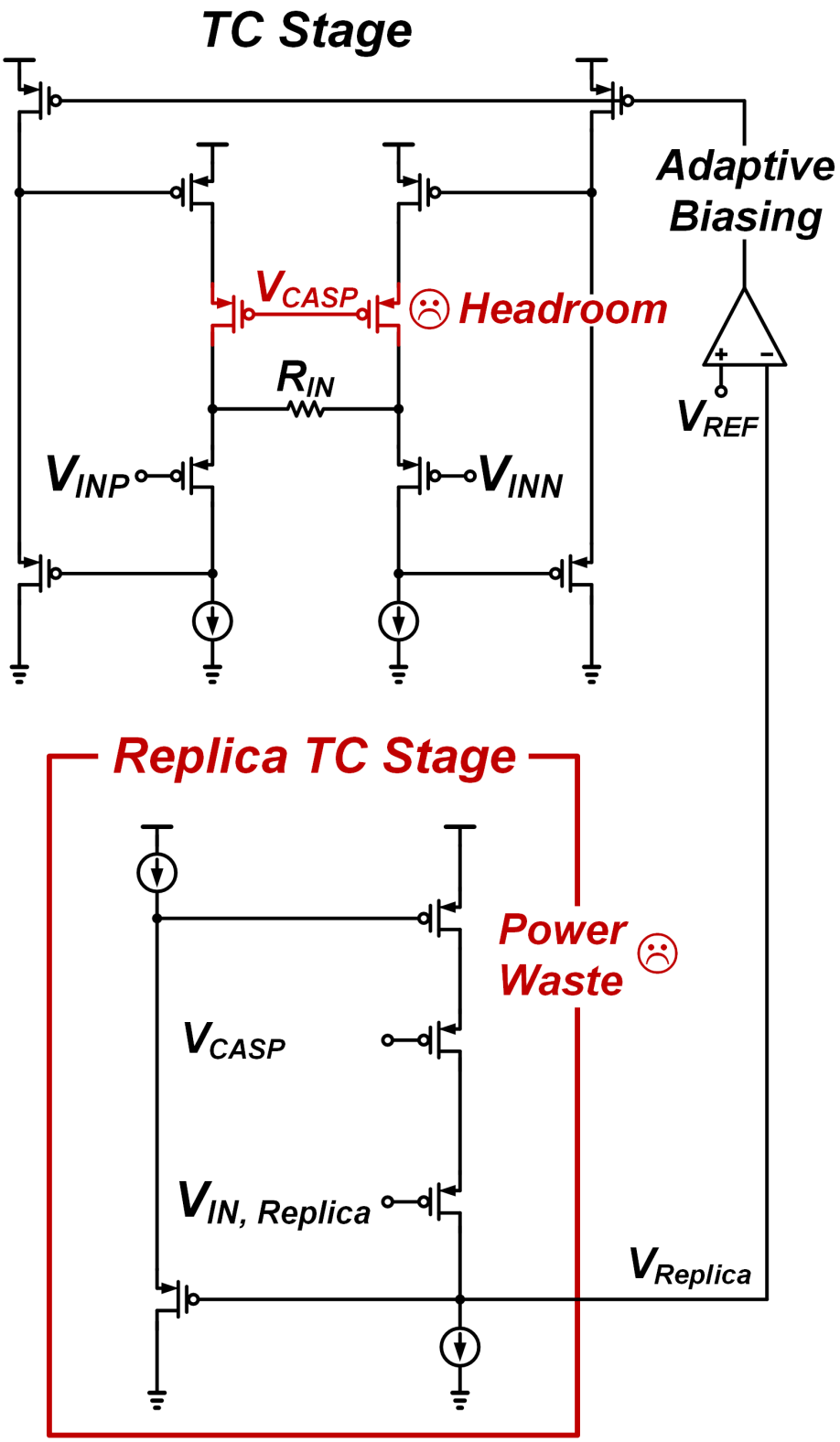

Figure 14. Limitations of previous current-feedback IA.

earlier FVF circuits in Figure 11(a)-(e), which used V_{GS} for drain node biasing of the input transistor and thus exhibited bias variations. In this article, pseudo-resistors [44] extract the CM signal and g_{m2} amplifier controls the amount of current of g_{m3} so that V_{GS} of g_{mff} can be V_{REFTC}, and the input transistor can be ensured to remain in saturation. This approach has two benefits compared with the conventional replica-based headroom improvement [27] as shown in Figure 14: 1) only a little additional current is required for g_{m2} amplifier (10 nA, Figure 15), instead of a power-hungry replica TC stage regarding that the TC stage typically consumes most of the IA power [39]; 2) much more stable BW performance over PVT variations because the adaptive biasing of g_{m3} should compensate only $1\times V_{GS}$ of NMOS (g_{mff}), not $2\times V_{SG}$ of PMOS. Note that the input transistors of g_{m2} amplifier are I/O devices, to avoid gate-leakage-induced resistance variation of the pseudo-resistors.

In addition, the proposed IA utilizes a proportional-to-absolute-temperature (PTAT)-compensated voltage reference in order to bias gate voltage of the input transistor through the front-end passive HPF, for the compensation of complementary-to-absolute-temperature (CTAT) property of V_{TH} [45]. The designed voltage reference is buffered by a unity-gain configured low-power operational transconductance amplifier (OTA), which is similar to g_{m2} amplifier. Hence, source node of the input transistor can be biased appropriately over PVT corners (290–390 mV) and it leads to a headroom improvement. Furthermore, it also improves headroom condition of the TI stage since source node of the input transistor is buffered to regulate current mirrors within the IA (TI_{Drain}). The TC stage is designed to have an only three-transistor stacking for all branches in order to further improve the headroom. This is achieved by utilizing midpoint node of the R_{IN} that is used as TI_{Drain} for

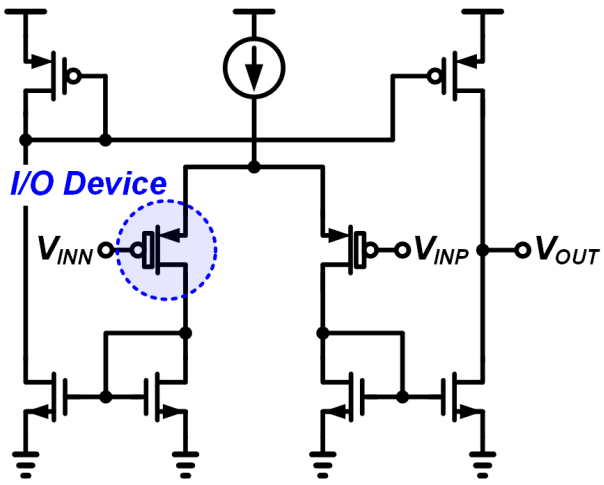

Figure 15. Current-mirror operational transconductance (OTA) used in g_{m2} amplifier of the IA.

drain regulation loop of current mirror in the TI stage, instead of cascode-based sensing [27]. Note that low-V_{TH} transistor design helps g_{mff} to be easily biased to a subthreshold region of V_{GS} around 125 mV (V_{REFTC}) and reduces V_{SG} drop of the other transistors ($g_{mR,m3}$).

Since the IA is a front-end circuit of the Bio-Z sensors, a low-noise performance is essential. As discussed in [27], R_{IN} should be designed as a low value because it is a dominant contributor to the overall IA noise performance. Therefore, the FVF with a GB loop, as shown in Figure 11(e), is more beneficial for a low-noise performance compared with the other FVF topologies since the loop gain degradation due to the low-valued R_{IN} can be mitigated [5]. However, as R_{IN} decreases, it leads to the different loop responses between the CM and the differential mode (DM) and makes the frequency compensation complicated, eventually resulting in

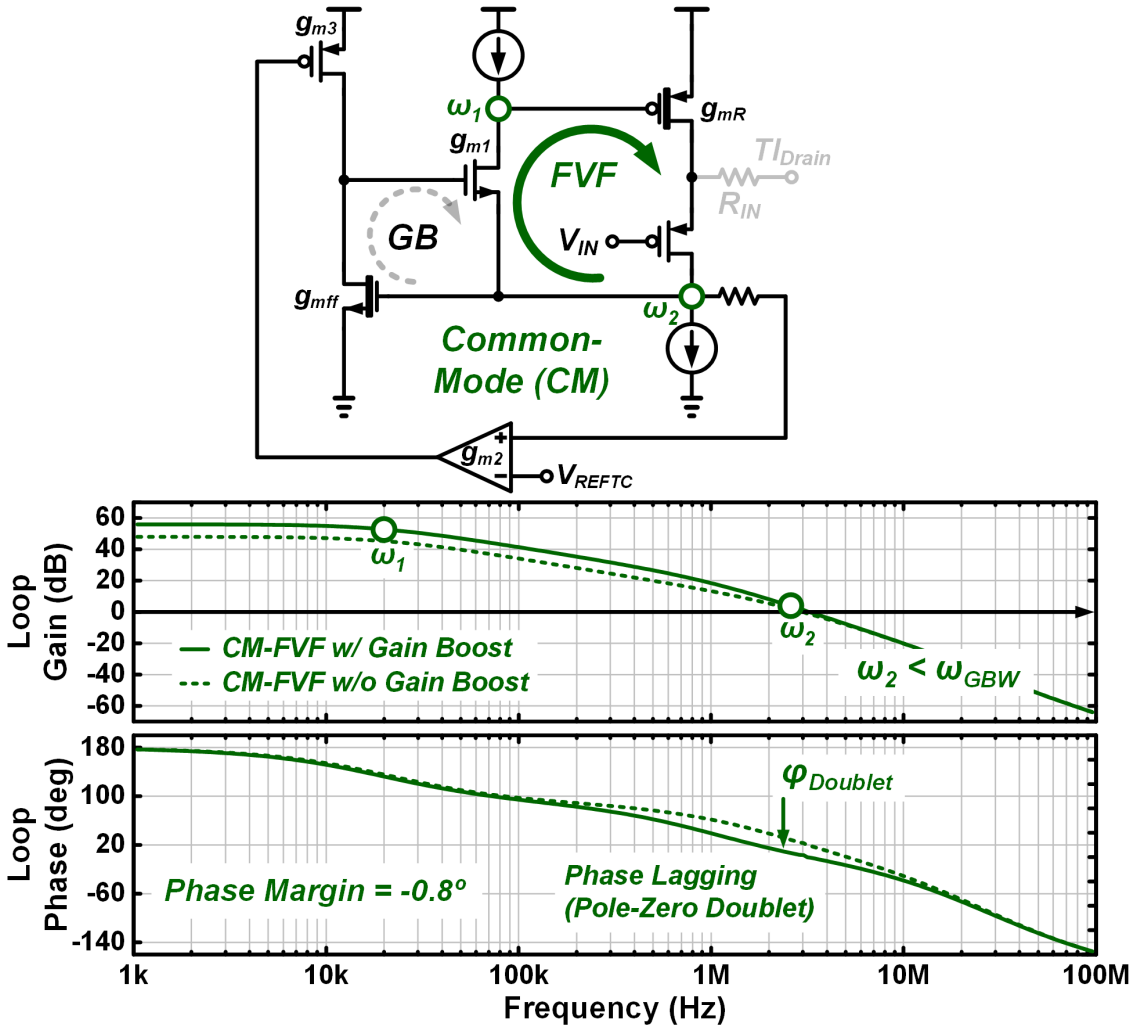

Figure 16. Half circuit representation of the TC stage for the CM loop condition with Bode plot for loop responses.

a limited BW performance. This is because R_{IN} forms a high impedance for the incoming CM signal but a low impedance (2 kΩ in this design) for the incoming DM signal.

Figure 16 and Figure 17 shows the FVF loop response for the CM and the DM conditions, with a half circuit representation of each case. ω_1 and ω_2 correspond to a dominant pole and a nondominant pole of the FVF loop, respectively. There are two major stability issues related to the CM-FVF loop response. First, as shown in Figure 16, the CM-FVF is required to be stabilized, showing a -0.8º of phase margin, whereas the DM-FVF (Figure 17) achieves a 46º of phase margin without any frequency compensation. The DM-FVF has its nondominant pole located higher than its GBW; on the other hand, the nondominant pole of CM-FVF is located

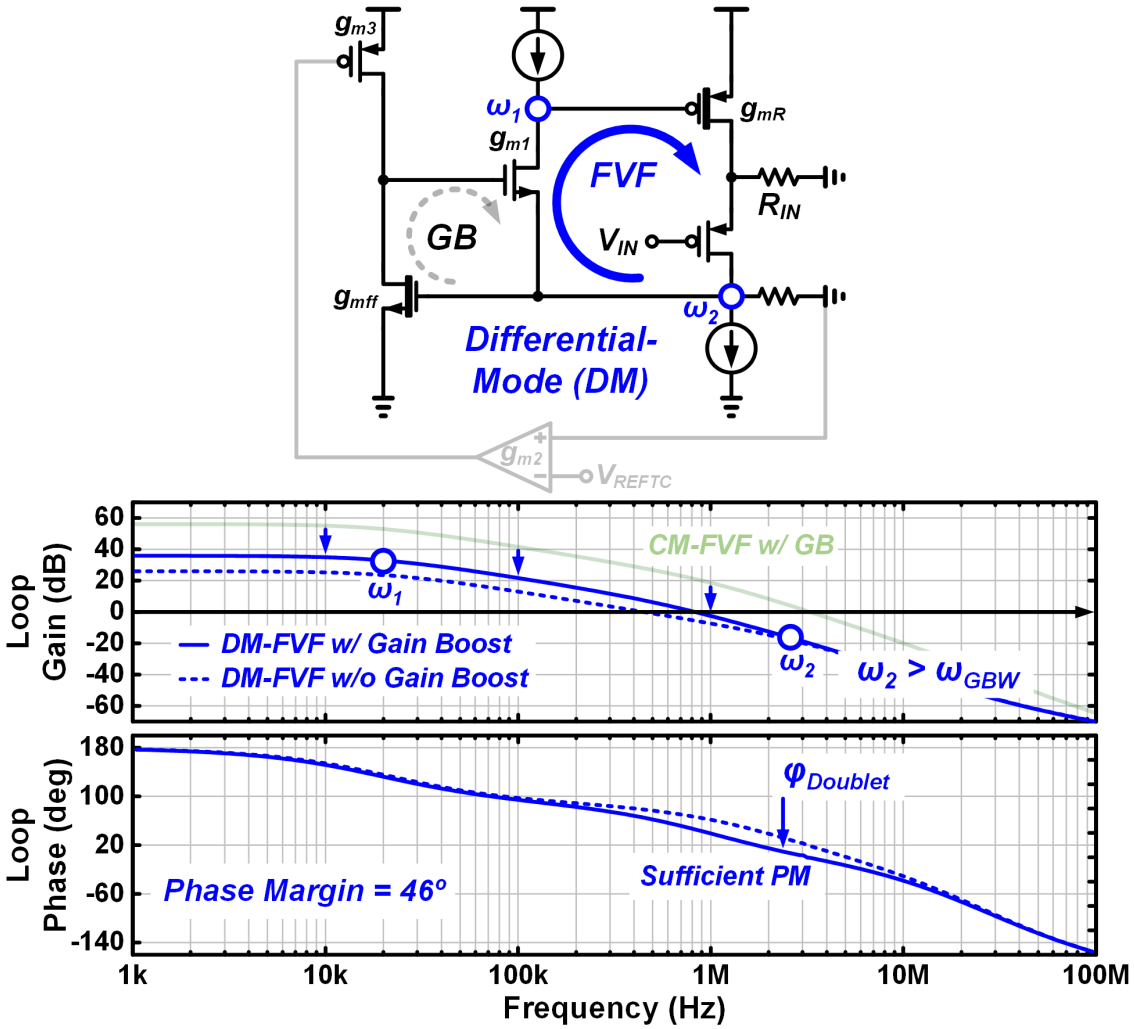

Figure 17. Half circuit representation of the TC stage for the DM loop condition with Bode plot for loop responses.

lower than its GBW. This is because the low value of R_{IN} effectively acts as an attenuation compensator for the DM-FVF, lowering its loop gain and GBW. Second, a temporary phase lagging effect arising from the pole-zero doublet due to the GB loop [42] further worsens the phase margin of CM-FVF loop. It can be expected through Figure 16 that the CM-FVF loop would have a 20º of phase margin without pole-zero doublet effect. Despite these challenges, the frequency compensation method of the previous design simply reduced the GBW of GB loop, resulting in an overcompensation of the DM-FVF loop. In [5], a Miller compensation was used so that phase lagging of pole-zero doublet occurs at a much lower frequency band than the GBW. However, this approach reduces not only GBW of the CM but also GBW of the DM, and thus, it resulted in an unnecessary GBW sacrifice of the DM-FVF loop. Since the GBW of the DM-FVF loop mainly determines the overall BW performance of the IA, the previous work did not provide an optimal solution for a wide-BW IA design.

Therefore, a lead-compensated TC stage is proposed. The frequency response of the lead-compensated TC stage for the CM-FVF loop response is shown in Figure 18. Since the lead compensation (LC) provides a capacitive bypassing that is a phase leading path, it compensates phase lagging of the CM-FVF allowing a zero insertion effect at the high-frequency band. By choosing the appropriate value for C_{LC}, the phase leading can be located around the GBW of the CM-FVF, which improves the phase margin. In this design, a 1-pF MIM

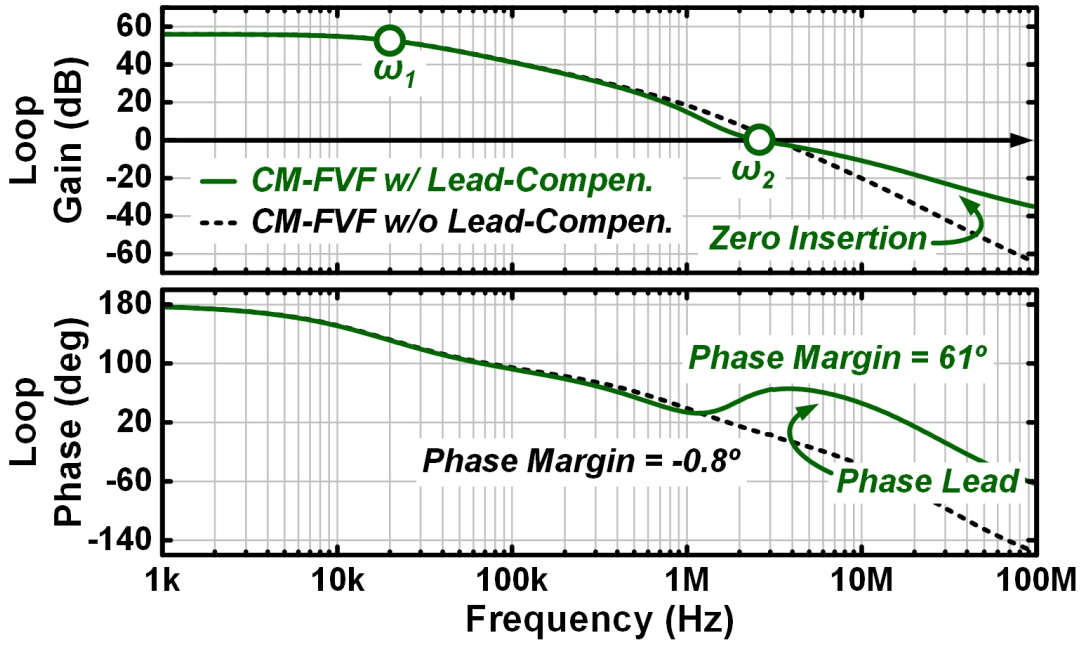

Figure 18. LC scheme of the TC stage for stabilization of the CM-FVF loop.

capacitor is used for CLC implementation. Figure 19 shows the DM-FVF loop response compared with the previous TC stage design [5]. Phase margin (PM) of the CM-FVF is set to 65º for a fair comparison (C_C). Since the LC does not utilize GBW reduction of the GB loop (C_m), it leads to a 5.85× higher GBW and an increased loop gain of 17 dB at a 20-kHz modulation frequency. For the CMFB loop stabilization that is three-stage feedback path (g_{m1}–g_{m2}–g_{m3} with g_{mff}), a nested Miller compensation with feedforward stage and nulling resistor (NMCFNR) is used [47]. Capacitances of C_{m1} and C_{m2} are minimized so that not to overcompensate the DM-GB loop, considering they are shunted to the virtual GND for the DM response.

3.1.2 Transimpedance Stage

Design strategy to maximize the BW of the overall IA is also considered in the TI stage. Unlike the previous works that located the demodulation step after the IA [5], [20], [40], choppers are implemented at low-impedance nodes of the TI stage as in [27]. This approach isolates high-frequency current signal from the output load of the TI stage, thus avoids BW degradation, and obviates the need for power consumption of the TI stage.

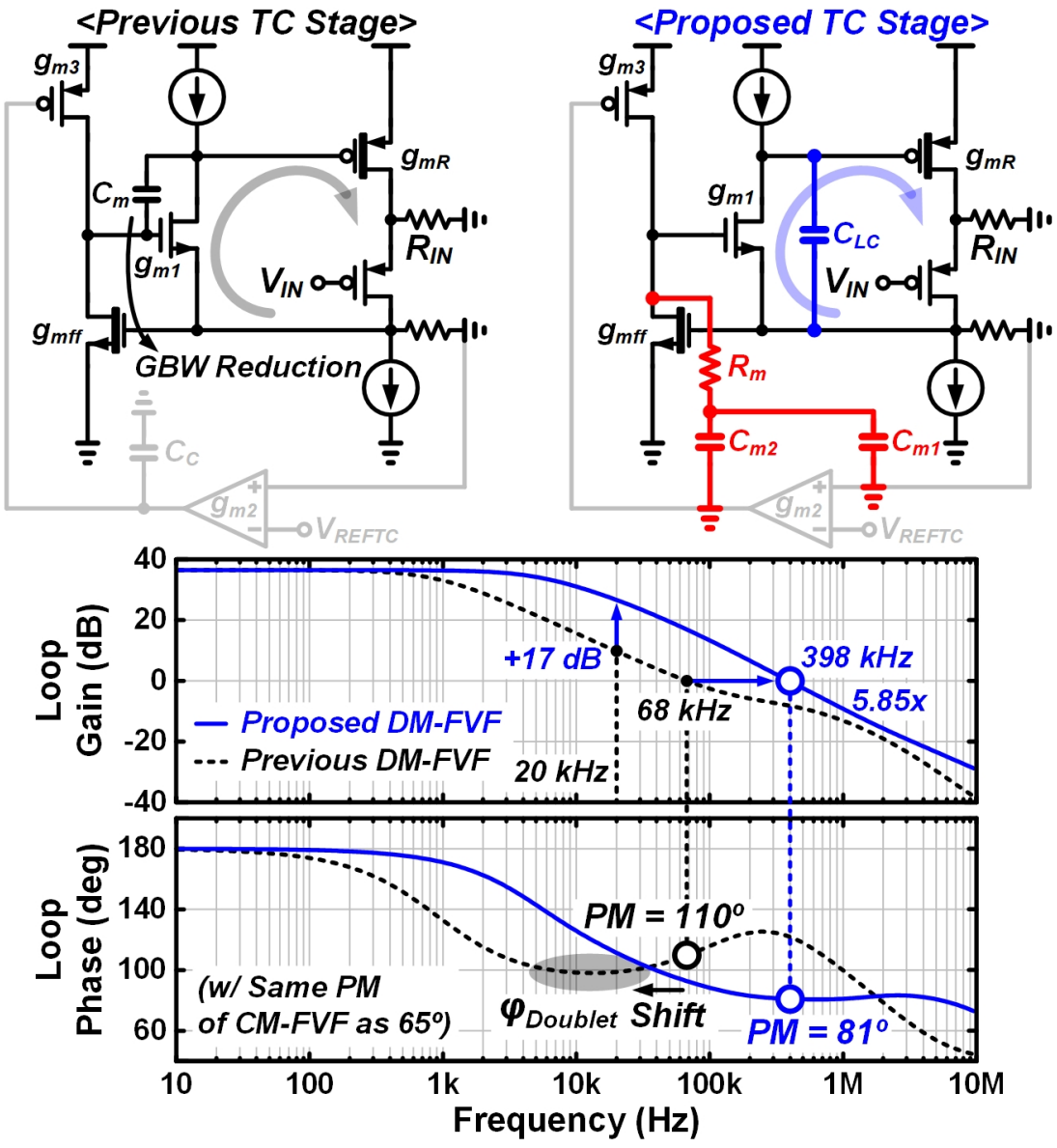

Figure 19. Lead-compensated TC stage compared with the previous TC stage for the DM-FVF loop response.

This is because the target BW of the baseband Bio-Z signal is <10 Hz. As a result, it allows an optimized distribution of power budget so that the TC stage can draw most of the IA power. The designed current mirroring ratio from the TC to the TI stage is set to 1/30, while the residual drain voltage mismatches are automatically corrected by a drain regulation loop, as shown in Figure 13. A Miller-compensated CMFB loop is used for the TI stage to provide $3V_{DD}/7$ (214 mV) of the output node biasing. Therefore, V_{DS} drop is allocated around 200 mV for current mirrors and 100 mV for each of the remaining transistors. Low-V_{TH} design and high-V_{TH} design are provided for improvement of headroom and enhanced loop gain of the CMFB loop, respectively.

3.2 Design of the 0.5 V V-I Converter

Conventional source-follower-based V–I converters [1], [6] suffered from a gain loss as a conversion resistor (R_{VI}) decreases. Hence, a large amount of bias current was required (2 mW in [1]) to buffer the input signals to R_{VI} without gain loss. An alternative method to achieve a low-power operation necessitates a design of R_{VI} up to MΩ range to accommodate μA bias current. However, it requires amplitude of the input signal to be

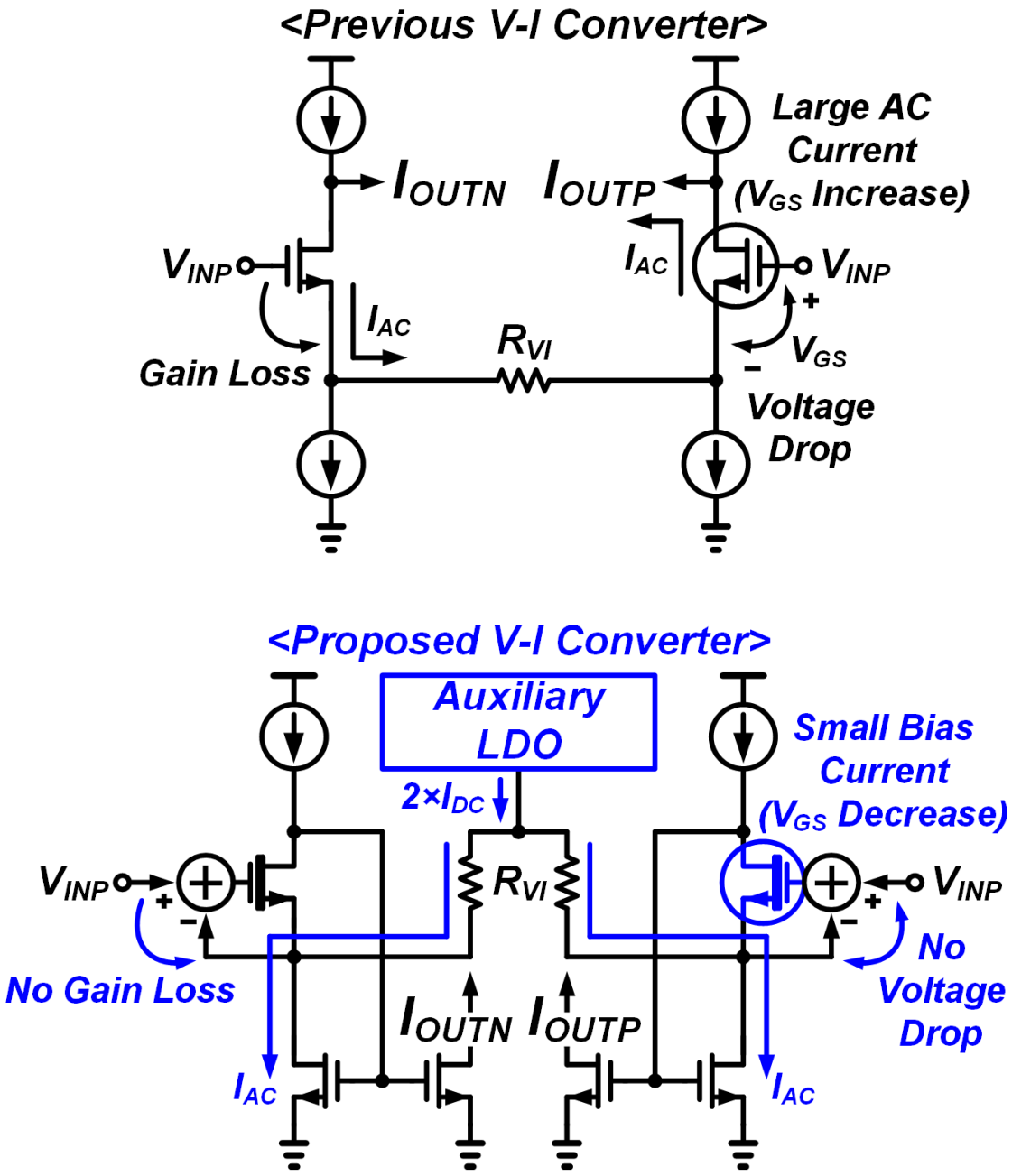

Figure 20. Conceptual diagram of LDO-based V–I converter compared with source-follower-based V–I converter.

increased proportionally, inevitably leading to a high supply operation. To achieve both a low-power and a low-supply operation, we propose an low-dropout regulator (LDO)-based V–I converter architecture that operates from a 0.5-V supply.

Features of the proposed LDO-based V –I converter are as follows, shown in Figure 20: 1) the input voltages are buffered to R_{VI} without V_{GS} drop and gain loss, by virtue of the LDO operation that enhances headroom and power efficiency; 2) the proposed auxiliary LDO supplies the required ac currents to the pass transistor obviating the need to bias a large current on M_{CS1}, and thus, V_{GS} of M_1 is reduced and headroom improves; and 3) residual dc currents ($I_{Residue}$) are rejected by the auxiliary LDO so that low-power operation is achieved.

Figure 21 shows the LDO-based V–I converter operating from a 0.5 V supply voltage. Two differential FVF LDOs similar to Figure 11(b) [48] are implemented for differential current generation so that even harmonics are canceled out. When the input signals are buffered to V_{2P} and V_{2N}, voltage difference across

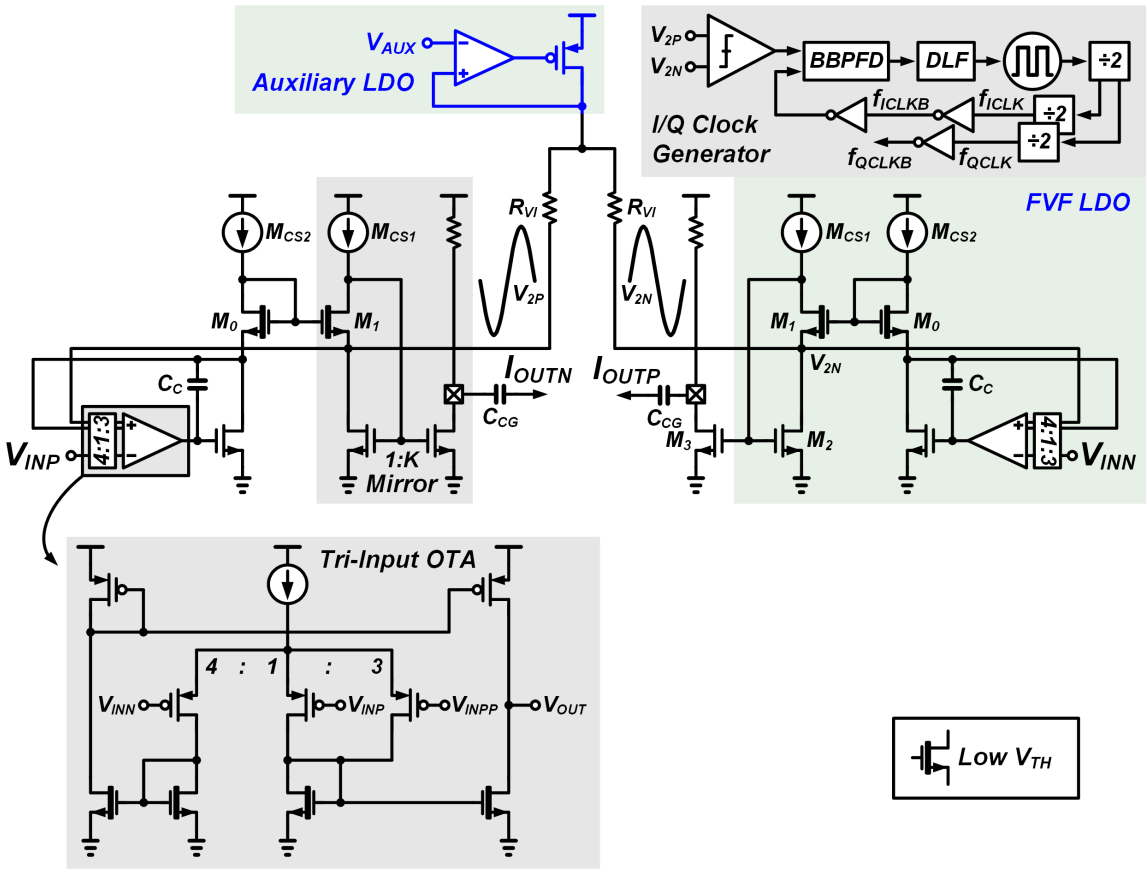

Figure 21. 0.5 V supply LDO-based V–I converter and I/Q clock generator.

a conversion resistor (R_{VI}) generates current signals that flow through a pass transistor (M_2). Since M_3 acts as a current mirror, ac current flows out of the chip and it is injected into the human body. This approach isolates the FVF loop from the parasitic effects of PCB and pads, and thus, loop stabilization is simplified. To deal with a current mirroring mismatch inherent in the FVF LDO, a tri-input OTA [48] is adopted, but it is implemented based on a current mirror OTA to maximize the output swing, rather than a five-transistor OTA design. As introduced in [48], since the tri-input OTA used in this design provides two buffered output ($V_{INP,\ INPP}$) of the input signal (V_{INN}) that are connected to each of source nodes of the current mirrors, both of positive pins can be corrected by virtue of the negative-feedback operation. The used low-V_{TH} transistor design enhances the headroom, which reduces V_{GS} of the diode-connected transistors of tri-input OTA. By the same token, $M_{0\text{-}1}$ are also designed in the low-V_{TH} transistor for a low-supply operation, and the designed output current of the V–I converter is fixed to a 8.4 μA_{pp}, which relaxes V_{GS} variation of M_2. Process variation of the output current is trimmed by a 2 bit digital control of R_{VI}.

Figure 22 describes the I Residue rejection using an auxiliary LDO. Since both the dc and the ac voltages are converted to the current by R_{VI}, $I_{Residue}$, which is an amount of current at the minimum point of the current signal, should be rejected for a low-power operation. Without the auxiliary LDO, R_{VI} should be connected to V_{DD}, which results in a residual DC voltage difference of $V_{DSAT,MCS1} + V_{DSAT,M1}$ on R_{VI}, and it leads to a 12.6 μA of power waste. When the proposed auxiliary LDO drives a predefined DC voltage (V_{AUX}) to R_{VI}, however, the residual DC voltage difference is reduced down to $V_{AUX}–V_{2,MAX}$. Using the V_{AUX} that is set to near the maximum swing level of V_2 ($V_{2,MAX}$), DC bias of the signal current is shifted and $I_{Residue}$ is rejected down to a 0.16 μA. Note that load current of the auxiliary LDO has only DC component since the differential AC current that flows through the R_{VI} cancels out each other. This rules out the light-load condition [48], which allows a simplified design of the fully integrated auxiliary LDO. Compared with the recently published V–I converter architecture that also deals with the $I_{Residue}$, the proposed LDO-based V–I converter has an advantage for low power since $I_{Residue}$ is simply separated from the ac current before it is mirrored in [36], rather than reducing its amount. As a result, 8.4 μApp of 20-kHz AC current is injected by the proposed LDO-based V–I converter, consuming only a 4.62 μW.

The implemented I/Q clock generator is based on a bang-bang digital PLL, as shown in Figure 21. Since the target locking frequency is 20 kHz that is very low to implement an analog loop filter, a digital loop filter (DLF) is utilized to allow an on-chip generation of the quadrature demodulation clocks to the IA. Note that the operating frequency of a digitally controlled oscillator (DCO) [49] is 4× higher than the I/Q output clocks: 2× for the duty-cycle correction and another 2× for a 90◦ phase shift generation between the I/Q clocks.

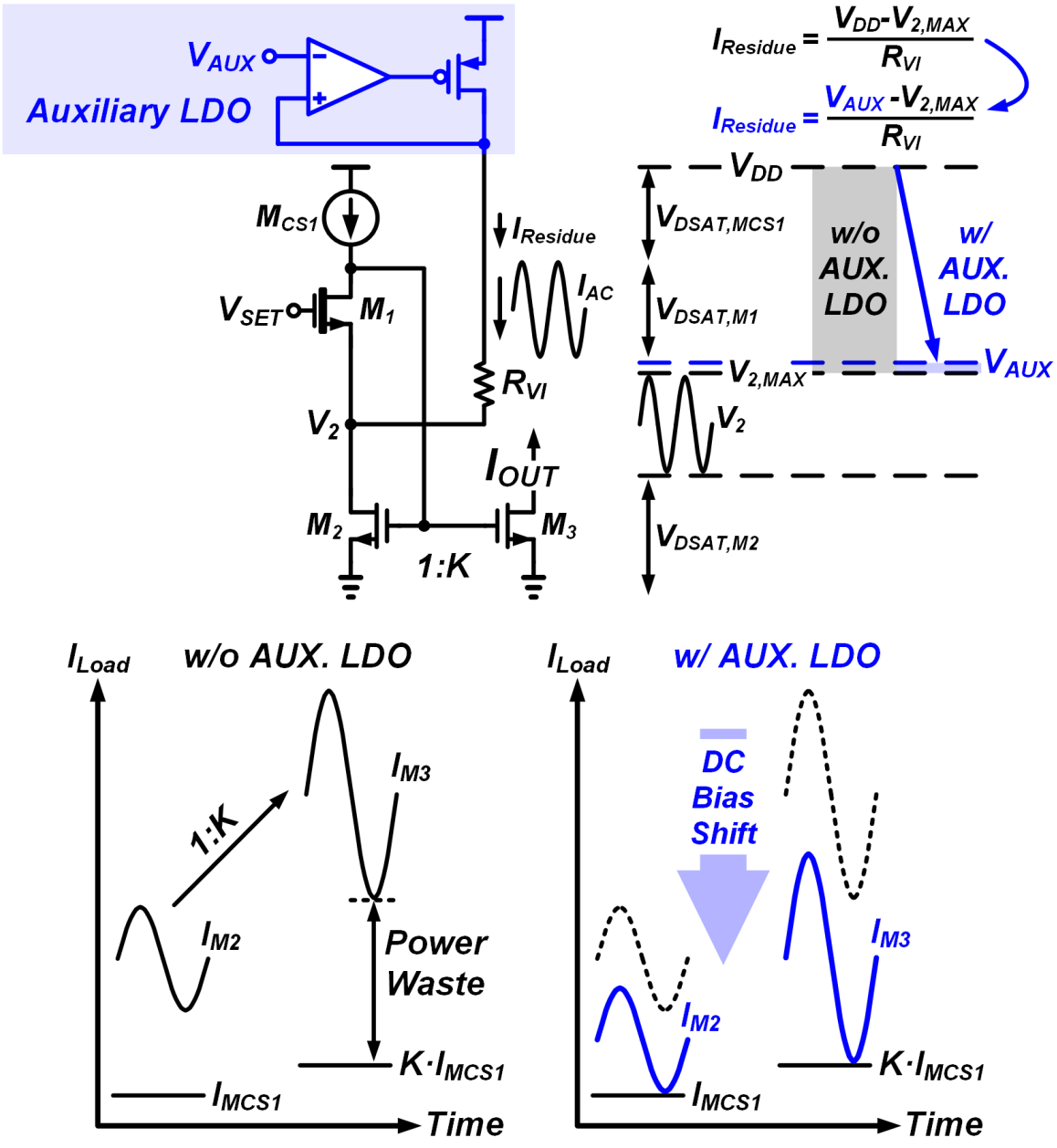

Figure 22. Conceptual diagram of $I_{Residue}$ rejection using auxiliary LDO.

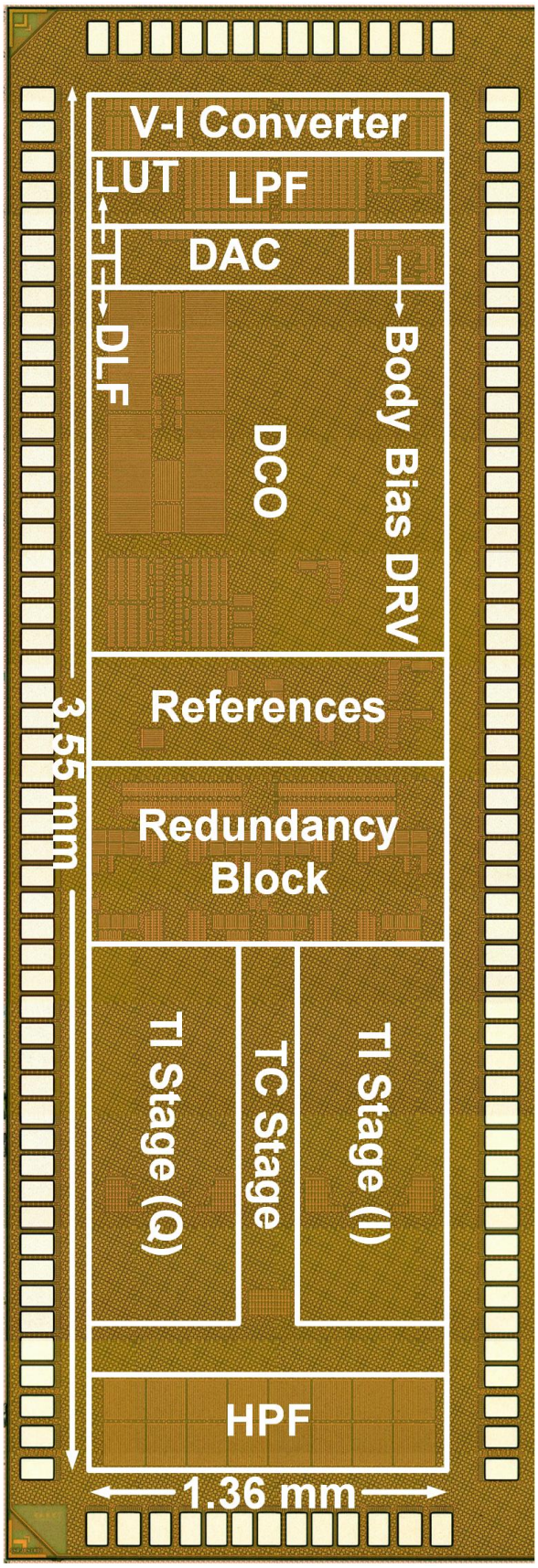

Figure 23. Chip micrograph of the proposed Bio-Z sensor IC which is fabricated using a 65 nm CMOS technology.

3.3 Implementation Results

The proposed Bio-Z sensor IC is fabricated in a 65 nm CMOS process with an area of 4.83 mm^2 (see Figure 23). In the measurement setup of the proposed Bio-Z sensor IC, a waveform generator of Keysight 33600A, a signal analyzer of Keysight 35670A, and an oscilloscope of Keysight 54845A and DSOX2024A are utilized.

The measured gain curve of the IA is shown in Figure 24. A 1 Hz sine wave that is amplitude-modulated with a kHz modulation frequency (1 mV_{PP} and 10% modulation depth) is applied to the input of the IA. Demodulation clock with the same frequency of modulation (kHz) is also provided by the waveform generator. The output of the IA is further amplified by an off-chip post-amplifier (AD8421) with a gain setting of 100×, and the fully differential output of the IA can be converted to the single-ended configuration, which

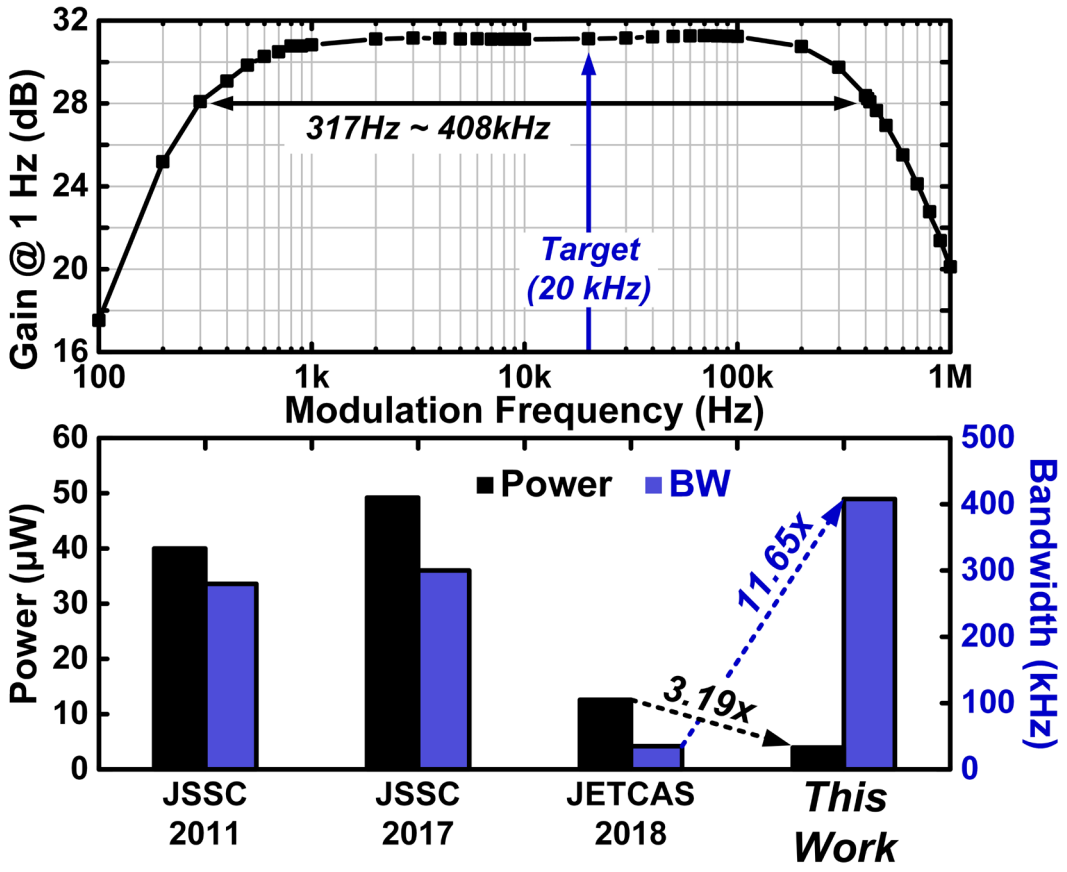

Figure 24. Measured gain curve of the IA and comparison of BW and power with the previous designs.

allows being measured using the signal analyzer. An off-chip second-order LPF with a 10-Hz cutoff frequency is also added after the post-amplifier, to filter out the demodulated high-frequency noise components as discussed in the early paragraphs of Chapter 2. When the output amplitude of the 1 Hz signal is measured, the gain of the IA can be derived through dividing it by the input amplitude of 1 Hz signal, which is a 100 μV_{PP} in this measurement setup. The BW of the IA is measured by sweeping the modulation frequency. It achieves a midband gain of 31 dB and a BW of 317 Hz–408 kHz. A comparison of the BW with the previous works is also shown in Figure 24 [1], [5], [50], [24]. The proposed IA outperforms the BW by 11.65× while consuming a 3.19× lower power compared with the recently published design. As discussed in Chapter 3.1, the main reason for this BW improvement stems from the three facts as follows: 1) demodulation at low-impedance nodes within the TI stage; 2) LC scheme to maximize the GBW of the DM-FVF loop; and 3) 0.5-V low-supply operation that enables to draw more currents, but consuming the same power.

Figure 25 shows the measured output waveform and the spectrum of the current generator. The output

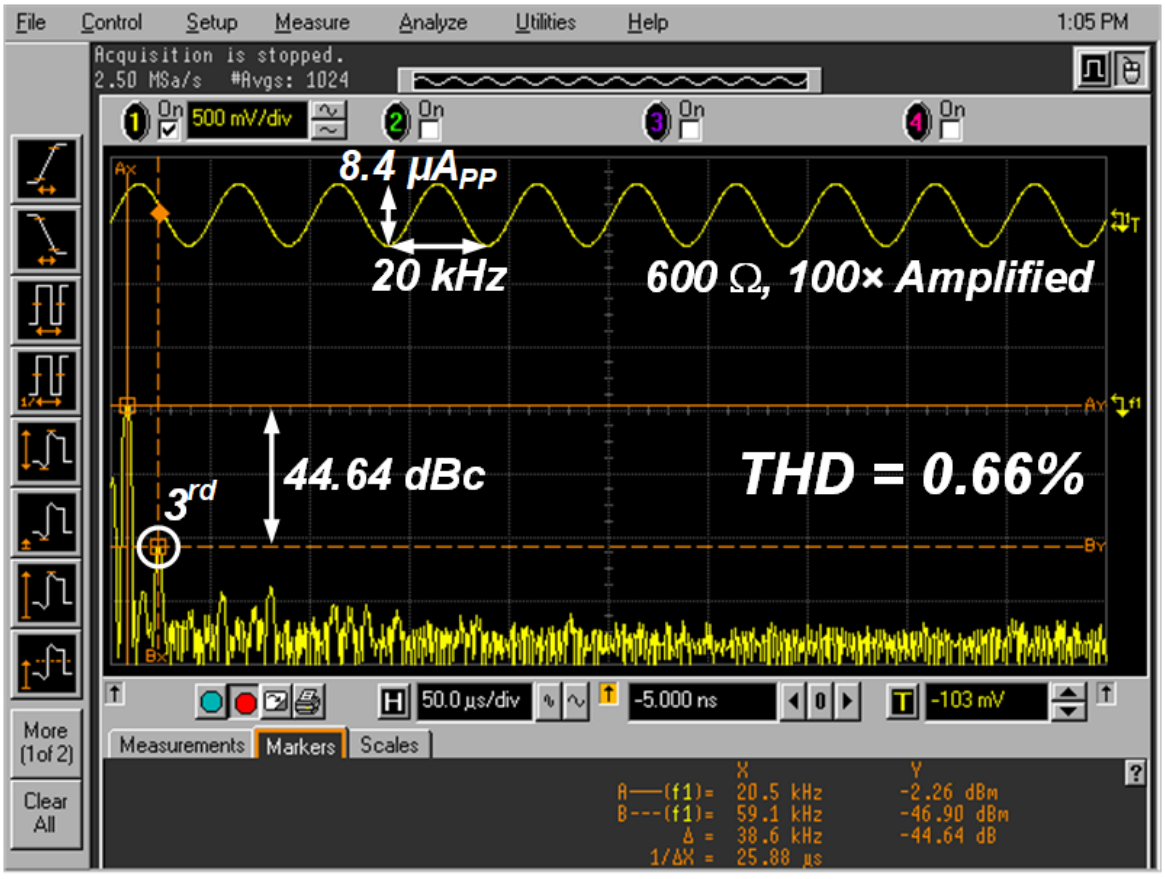

Figure 25. Measured output waveform and spectrum of the current generator.

sinusoidal current is applied to a 600 Ω of test resistor, and the resulting voltage signal is amplified by a 100× using AD8421, before it is sensed by the oscilloscope. The measured THD is a 0.66% with a 44.64 dBc of the spurious-free dynamic range (SFDR) when a 20 kHz and 8.4 µApp current is injected.

Figure 26 shows the measured spectrum of the overall input referred impedance noise and the measured overall phase error of the proposed Bio-Z sensor IC. Signal analyzer is used for the noise and phase error measurement, and the output of the IA is configured the same as the measurement setup of the gain and the BW (post-amplifying, low-pass filtering). To include the noise contribution of the current generator [13], [23], the sinusoidal output current of the current generator is applied to the test resistor of a 100 Ω and the voltage is sensed by the IA. When the output noise spectrum is divided by the gain of the IA (Fig. 14), the post-amplifier, and the RMS amplitude of the current generator output current as discussed in Chapter 1.2.1, the input referred impedance noise spectrum of a 15.28 mΩ/√Hz is obtained at 1 Hz. The phase error is measured over a 10% of

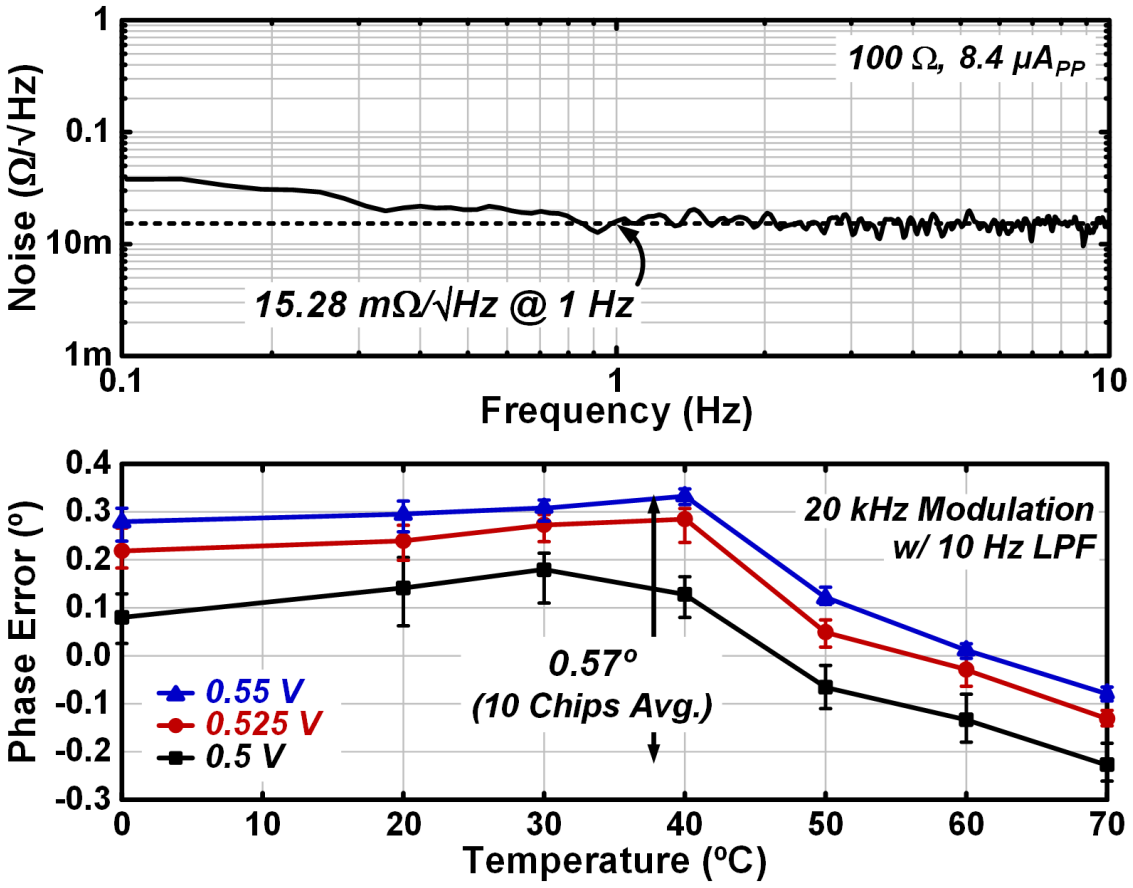

Figure 26. Measured input-referred impedance noise and phase error over temperature and supply variations.

supply and a 0ºC–70ºC of temperature variations with a 20 kHz modulation frequency based on the Equation (18). A 100 Ω test resistor is used. After a one-point calibration procedure, the maximum and the minimum value of a 0.59º and a 0.51º are achieved, while the average value shows 0.57º over ten chip samples.

Figure 27 shows the measured linearity performance. The proposed Bio-Z sensor IC can detect the purely resistive load with a maximum error of 2%, in the range up to 126 Ω. It is compatible with the required input range (<107 Ω) of the fluid status monitoring algorithm (OptiVol [7], [10]) that is clinically available on the implantable intrathoracic impedance monitoring devices. Degradation of the measurement capability over 126 Ω is mainly due to the limited input range of the IA (1.6 mV_{PP}). To validate the linearity of this IC for the various phase conditions, load impedance is configured to a purely resistive load, which is paralleled with a capacitor. When the capacitor value is changed, it generates a corresponding phase shift that can be detected by the proposed sensor IC. This measurement setup models the biologically relevant phase range of the CHF

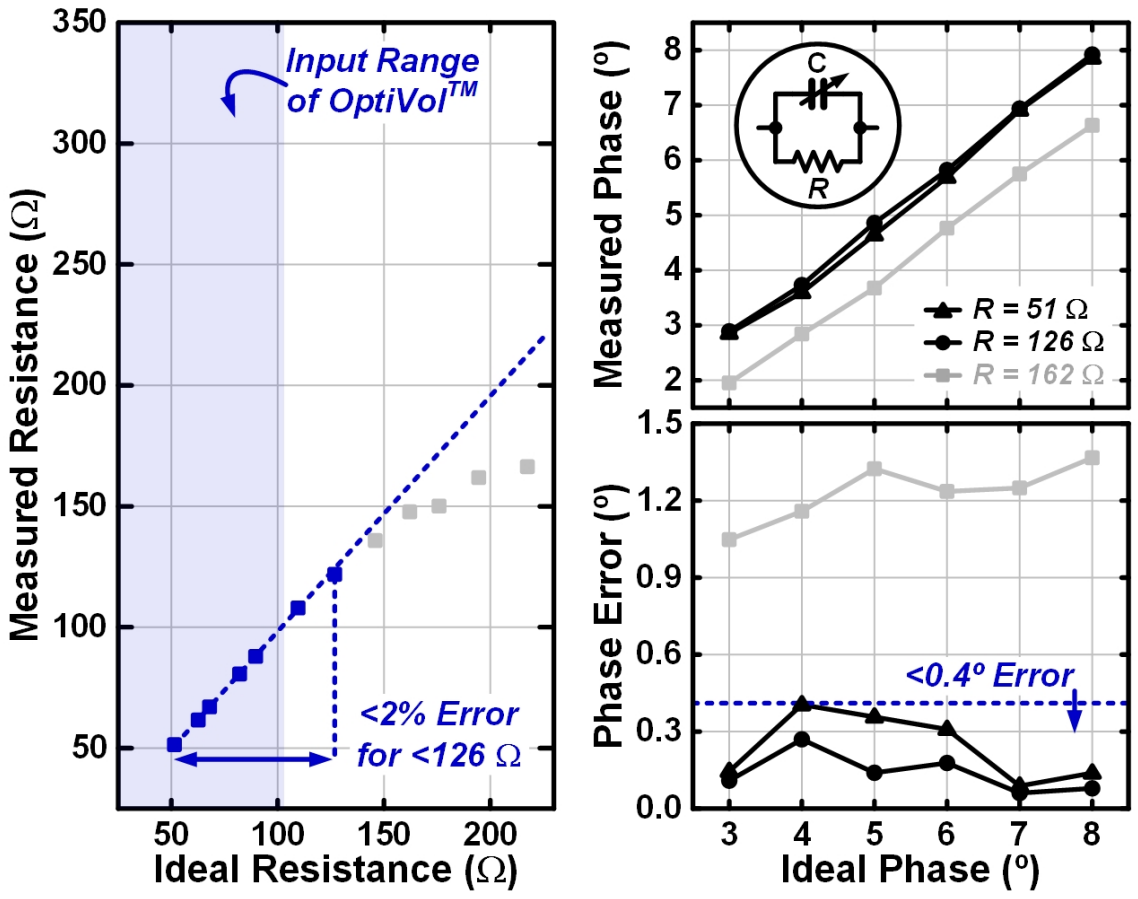

Figure 27. Measured linearity versus resistance and phase.

patients under the several tens of kilohertz range [8], [12]. As shown in Figure 27, this sensor IC can detect the phase shift of load impedance with the maximum error of 0.4º, given that the purely resistive component is below 126 Ω range. As expected in the linearity test of purely resistive load condition, phase linearity also starts to degrade showing larger than 1º of phase error when the paralleled resistance value exceeds 126 Ω.

The proposed Bio-Z sensor is also validated by an experimental measurement on the human chest (see Figure 28). Five electrodes are used for the measurement, including one for the body biasing and four for the tetra-polar configuration. An off-the-shelf evaluation board of MAX30001EVSYS (Maxim Integrated), which also has the Bio-Z acquisition capability, is adopted for the comparison of measurement waveform. Both the measured waveforms are low-pass filtered by a 4 Hz cutoff frequency [13]. As shown in Figure 28, it can be

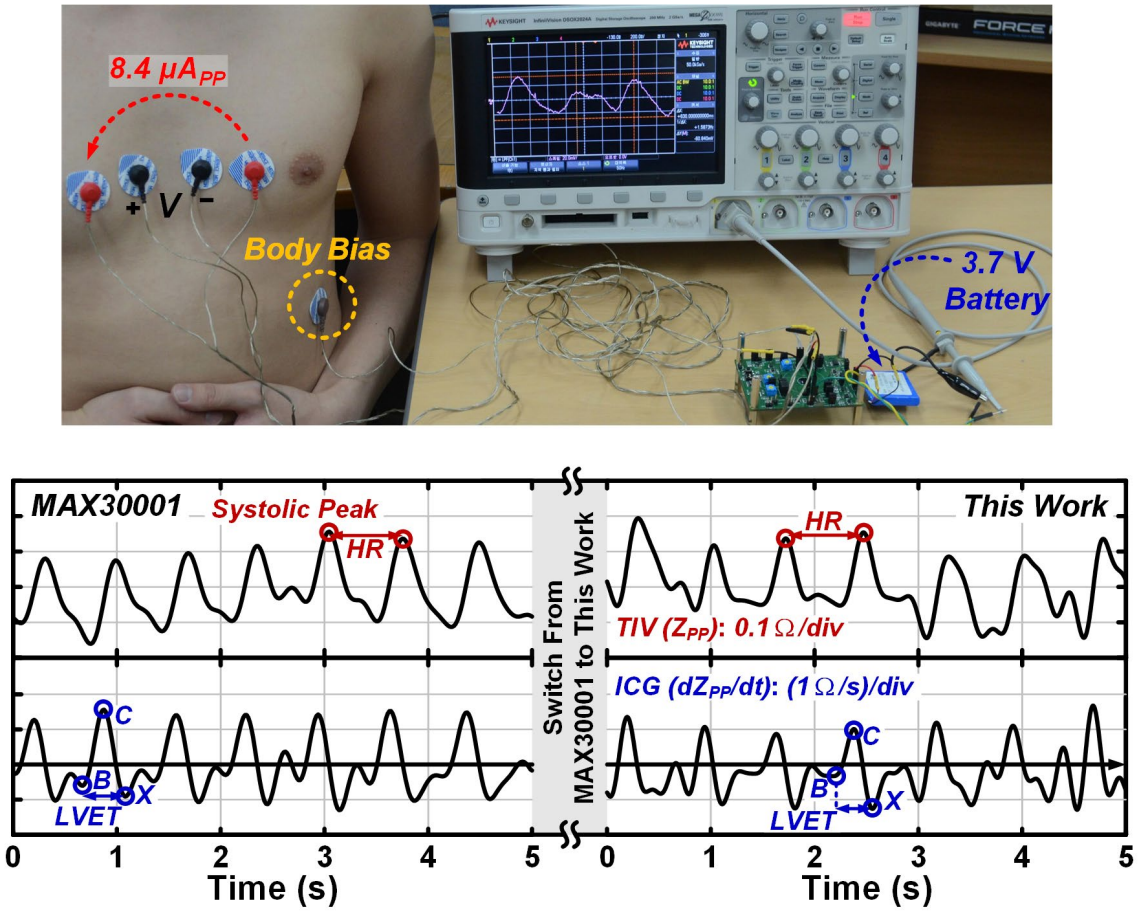

Figure 28. Measurement environment of the experimental test for the proposed Bio-Z sensor IC (upper photograph) and the measured waveforms of TIV/ICG (right). During the measurement, connections from the electrodes are switched from the MAX30001 to the proposed sensor IC, where the positions of electrodes are not changed. A 18 kHz and a 32 μA$_{PP}$ injection current is used with the MAX30001. The Bio-Z data measured from the MAX30001EVSYS are acquired through a laptop.

seen that the measured TIV/ICG waveforms using the proposed Bio-Z sensor IC are quite similar to the measurement using MAX30001. The waveforms of the TIV that is down to 200 $m\Omega_{PP}$ and the ICG are successfully monitored, showing the important points such as systolic peak of the TIV and B, C, and X-points of the ICG. Heart rate (HR) and leftventricular ejection time (LVET) are also extracted. Although this experimental measurement is not performed on the target environment of an implantable condition, the capability of the proposed Bio-Z sensor is verified in practice, with a given resolution specification.

Table I summarizes the comparison table and the graphical representation of comparison, including the state-of-the-art low-power (<100 μW) Bio-Z sensor ICs, is shown in Figure 29. The proposed Bio-Z sensor IC features the first 0.5 V lowest supply operation, which leads to an ultralow power of 9.26 μW. Considering the relationship of the noise (resolution) that is inversely proportional to the injected amount of current (power), it is clearly shown that none of the previous Bio-Z sensors have broken the borderline of power–noise tradeoff simultaneously satisfying <10 μW power and <50 mΩ/√Hz noise performances. Due to the 0.5 V low supply

Table I. Performance Summary and Comparison of the Bio-Z Sensor IC

	TBioCAS '13 [3]	JSSC '15 [16]	JSSC '15 [26]	VLSI '17 [17]	ESSCIRC '17 [15]	CICC '17 [18]	TBioCAS '18 [47]	AD5933	*This Work*
Technology (nm)	180	180	110	180	180	40	180	-	***65***
Supply (V)	1.8	1.2	1.2	1.2/1.8	1.8	0.6	1	3.3	***0.5***
Modulation Waveform	Pseudo-Sine	Pseudo-Sine	Square	Square	Pseudo-Sine	Square	Semi-Ramp	Pseudo-Sine	*Pseudo-Sine*
Modulation Freq. (kHz)	20	20	64	1-1024	20	32	2	1-100	***20***
Modulation THD (%)	0.7[A]	<4	-	-	1.78	-	-	0.25	***0.66***
Modulation Amp. (μA_{PP})	40	27	250	20	26	20	1	-	***8.4***
Phase Measure	Yes	Yes	No	Yes	No	No	Yes	Yes	*Yes*
Phase Error (°)	-	-	-	-	-	-	-	<0.8° (0°-7°)[B]	***<0.4° (3°-8°), <0.57°[C]***
Noise (mΩ/√Hz)	10.58[D]	9.8[D]	1.7[D]	3.84	12.49[D]	35	429[E]	-	***15.28***
Total Power (μW)[F]	56.16	58	392	81.7	24	15.78	1.55	33000	***9.26***

[A]THD after demodulation [B]Estimated from datasheet [C]Over supply & temp. variations
[D]Excluding CG noise [E]Estimated from RMS accuracy/√(0.1Hz-10Hz)
[F]Including CG & Current injection power

and the noise-BW-efficient design of the IA, this IC first meets the power–noise requirements of an implantable cardiac monitoring device, with a 15.28 mΩ/√Hz noise performance. Furthermore, it shows the lowest phase error performance, which is suitable for continuous fluid status monitoring applications.

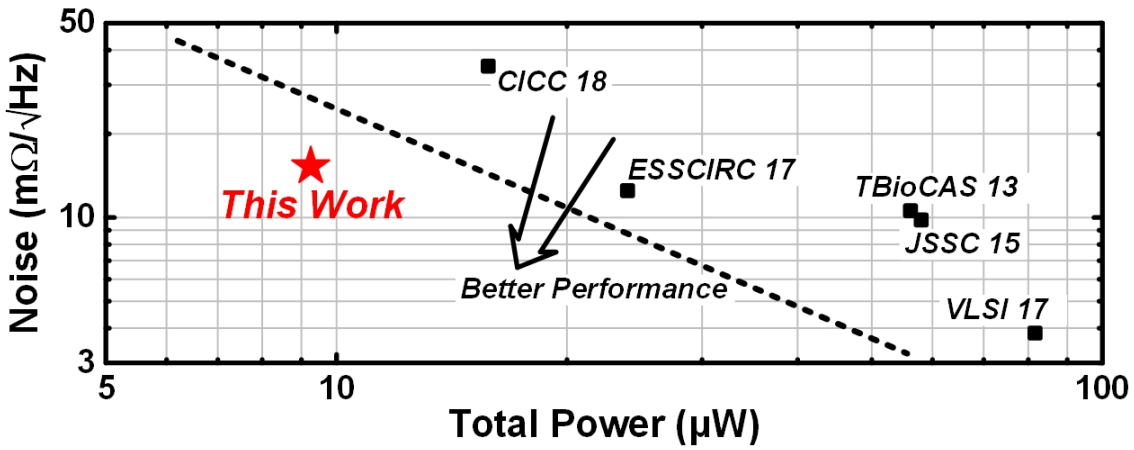

Figure 29. Comparison graph of the Bio-Z sensor ICs.

Chapter 4. Low-Harmonic-Distortion Sinusoidal Current Generator IC

In this Chapter, the first sub-10 μW, sub-0.1% total harmonic distortion (THD) sinusoidal current generator (CG) IC that is capable of 20 kHz output for the Bio-Z sensing applications is presented [51]. In order to benefit from the ultra-low-power nature of the near-threshold operation, a 9 bit psuedo-sine look-up table (LUT) is 3 bit ΔΣ modulated in the digital domain, thus linearity burden of the DAC is avoided and only a 1.29 μW of logic power is consumed, from a 0.5 V supply and a 2.56 MHz clock frequency. A half-period (HP) reset is introduced in the capacitive DAC, leading to around 30dB reduction of in-band noise by avoiding the sampling of data-dependent glitches.

CG of the Bio-Z sensor is an essential building block since the Bio-Z is modulated into a voltage waveform by an injection current, so that it can be sensed by a voltage readout circuit. As a simple and low-power method of demodulation as discussed in Chapter 2, chopping technique has been usually utilized in the voltage readout chain of the Bio-Z sensors, which in turn, eventually necessitates a low-distortion sinewave of the CG. For example, <1% of THD performance after chopping was used for the implantable pacemaker [2], [3] while even much tighter THD of <0.5% at the CG output was desired for the accurate electrical impedance tomography (EIT) applications [4]-[6]. Yet, the generation of low-distortion (<0.5%) sinewave has consumed a high-power (>50 μW) in the prior arts [5], [35], limiting the use of ultra-low-power applications (e.g. implantable) due to the severe lifespan reduction.

The presented CG IC has key specifications of 6.2 μW of power consumption, 0.059 mm^2 of active area, and 0.088% of THD with 20 kHz and 2 μA_{PP} injection current. Its low-distortion (THD) outperforms the recently published sub-10 μW Bio-Z sensor IC [29], [30] by 7.5×, which is discussed in Chapter 3, also exhibiting 8.9× less power consumption compared to the recently published sub-0.5% THD sinusoidal CG circuit [35] at the same time. In addition, its compact chip area compared to the other sinusoidal CG ICs allows the low-cost production. Graphical representation of its key performances are summarized and compared with the state-of-the-arts [1], [3]-[5], [30], [35], [36] in Figure 30.

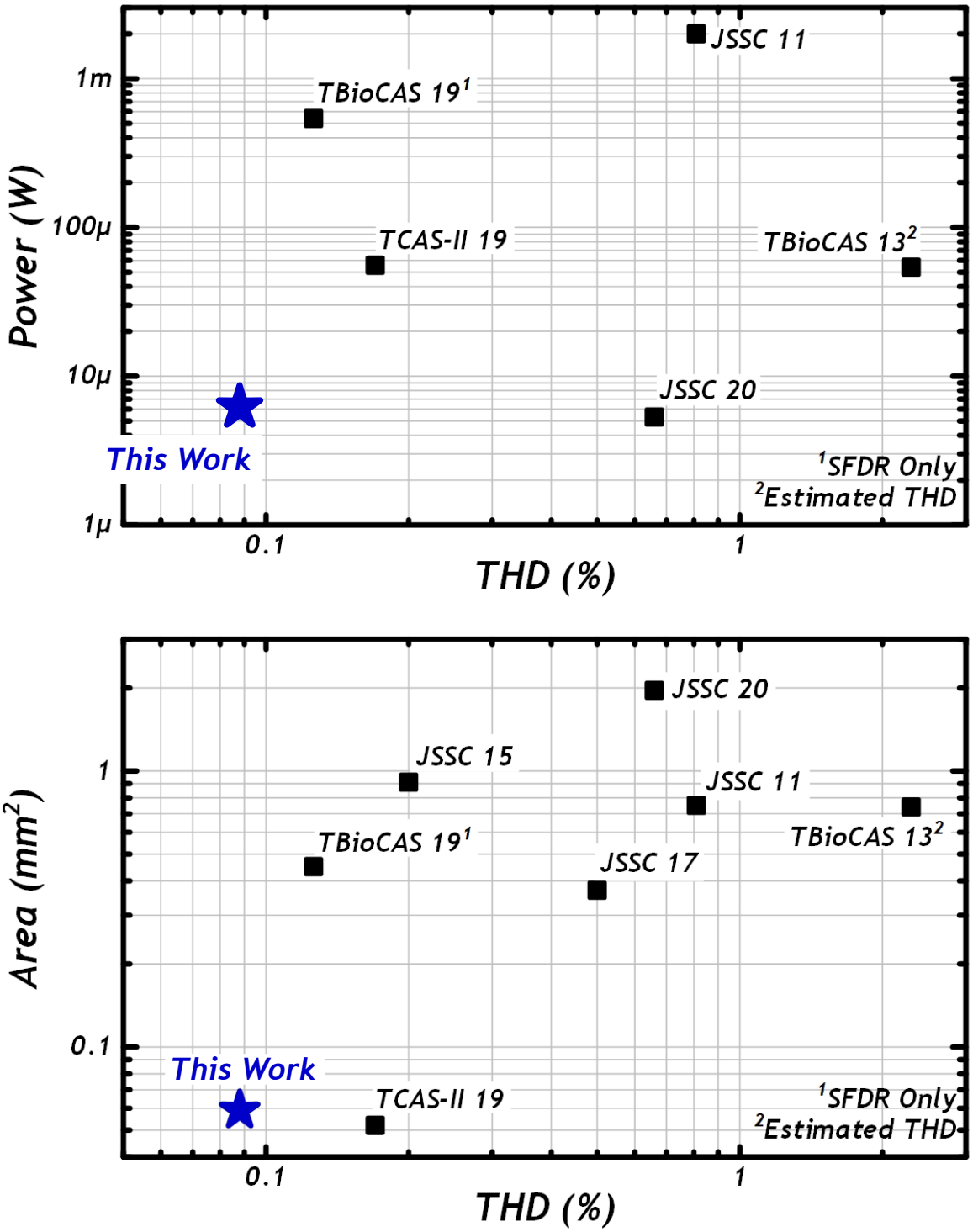

Figure 30. Comparison graph of the sinusoidal CG ICs.

The overall architecture of the proposed low-distortion sinusoidal CG IC is shown in Figure 31. It includes digital/analog parts of building blocks all of which are fully operating in a low-supply voltage of 0.5 V.

The digital part consists of a 9 bit pseudo-sine LUT, a 3rd-order digital multi-stage noise shaping

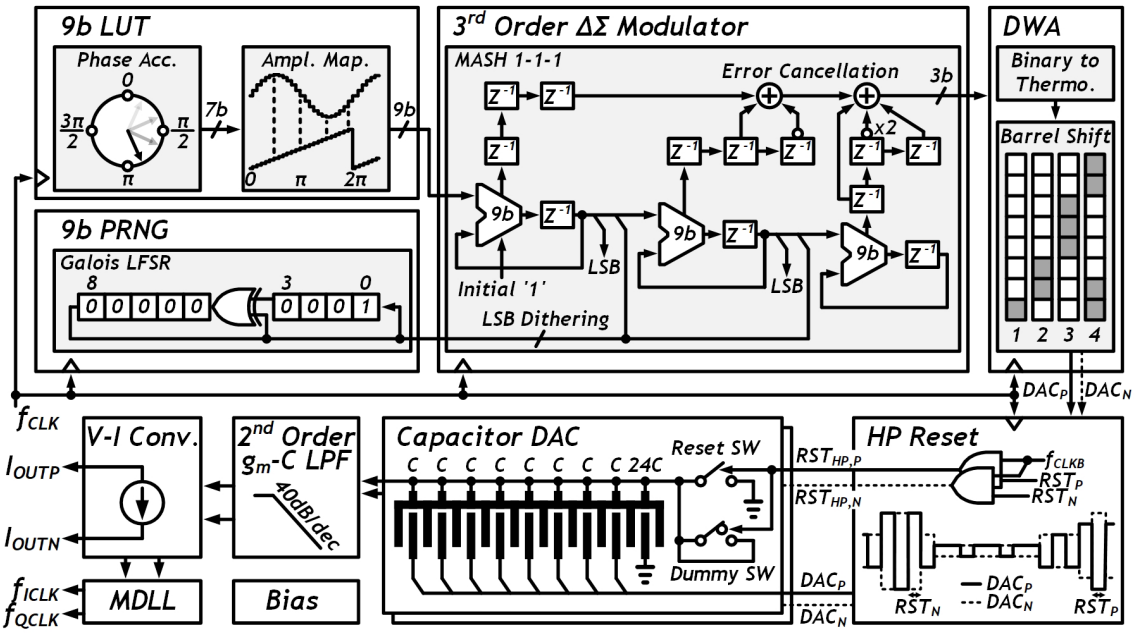

Figure 31. Overall architecture of the sinusoidal CG IC.

(MASH) 1-1-1 ΔΣ modulator, a 9 bit pseudo-random number generator (PRNG), and a data weighted averaging (DWA). When the phase accumulator sends a 128× rotational counter values to the amplitude mapped memory, the LUT outputs a 9 bit integer-numbered sinewave data. Then the ΔΣ modulator reduces the output bit-width of the digital part, to only a 3 bit, utilizing the carry-out property of digital accumulators. So it can lead to a low-complexity, and a power-efficient implementation. Furthermore, the designed PRNG reduces the pattern-spurs of digital ΔΣ modulator, and the DWA noise-shapes the mismatch of the DAC, using the barrel-shifting pattern.

The analog part consists of a 3 bit capacitive voltage DAC, a 2nd-order g_m-C LPF, and a V-I converter. Especially in the capacitive DAC block, a half-period reset scheme is proposed, and it allows the glitch-free sampling operation of reset switches within the DAC part, reducing the in-band noise floor. The final stage of the CG IC is V-I converter in which the generated low-distortion sinewave signal is converted into the analog current output, with the help of LPF.

This Chapter is organized as as follows. Chapter 4.1 discusses limitations of the previous sinusoidal CG ICs. Chapter 4.2 and Chapter 4.3 introduces the implementation details of the proposed CG IC. Chapter 4.4 shows the chip measurement results and performance summary.

4.1 Limitations of the Previous Sinusoidal CG ICs

Figure 32 shows the architectures of the previously reported sinusoidal CG ICs [1]-[5]. Although the RC-OSC-based sinewave generator as shown in Figure 32(a) proved its low-THD performance of <0.2% [1], [4], it consumed larger than 100 μW sorely for the sinewave generation, because the analog OTA requires a wide-bandwidth and a high-gain, resulting in power-hungry condition. On the other hand, a digital-analog mixed-signal implementation, using a sinewave LUT and a thermometer-coded current DAC, avoids analog OTA and it can achieve a low-power operation [2], [3], [5], [35]. The major challenge here to achieve sufficient spur reduction is the linearity burden of the DAC because of its typically thermometer-coded method in order to

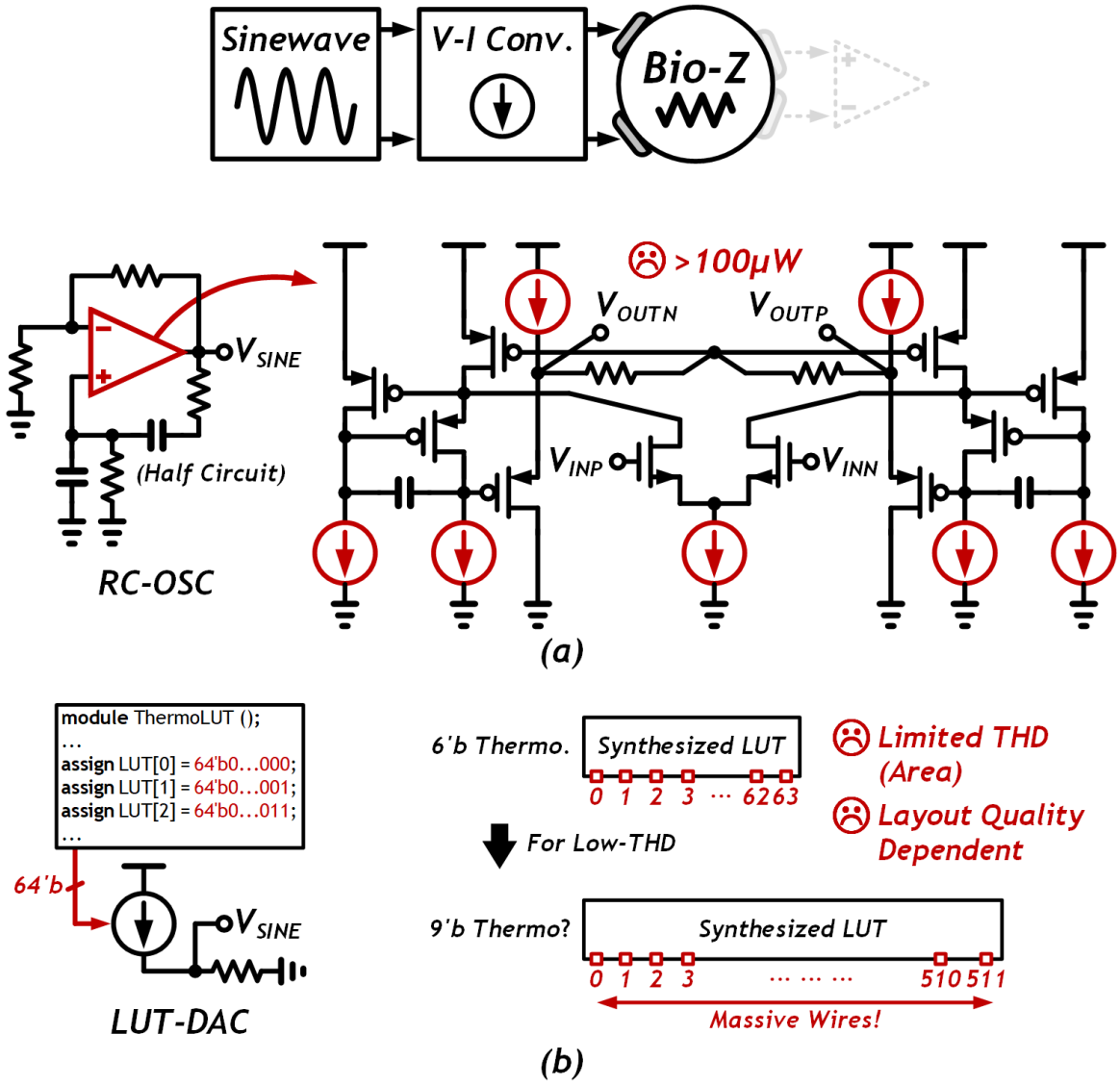

Figure 32. Limitations of the previous sinusoidal CG IC.

reduce the level-dependent glitches and matching requirements of the DAC. However in this case, the achievable THD performance is rather limited, because of its significant routing burden between the LUT and thd DAC (512 wires for 9 bit LUT as used in this work), leading to a large area occupation not only due to the massive wires but also due to the pin allocation of LUT during the logic synthesis, and also DAC itself. In addition, its THD performance is highly dependent on the quality of analog layout.

4.2 Design of the Digital Sinewave Synthesizer

To tackle the design issues as discussed above, this work adopts a digital ΔΣ modulation to the output of the LUT as shown in Figure 33. Therefore, there's no need to encode sinewave data into the thermometer-method, thanks to the fully digital interface. And, it results that even though the resolution of sinewave data is increased, it negligibly impacts chip area increase. Furthermore, the input bit-width of the DAC is highly relaxed to a 3 bit thermometer-coded, resulting in a significant area and design complexity reduction in both of the digital part and the DAC part. To reduce the power consumption of the entire chip, we apply a 0.5 V of low-voltage to benefit from the power-efficient near-threshold nature of the digital logic as much as possible.

Last but not least, the performance of this design is independent from the layout quality, by utilizing dynamic element matching. As a main focusing-point of the proposed CG IC stems from *decoupling* final performance of the sinusoidal waveform and the layout quality depending on the human experience, this approach can be expected to have a viewpoint towards the fully synthesizable design automation from the behavioral description to the layout generation [52]-[54], which has been already widely facilitated by the recent digital VLSI implementations up to now.

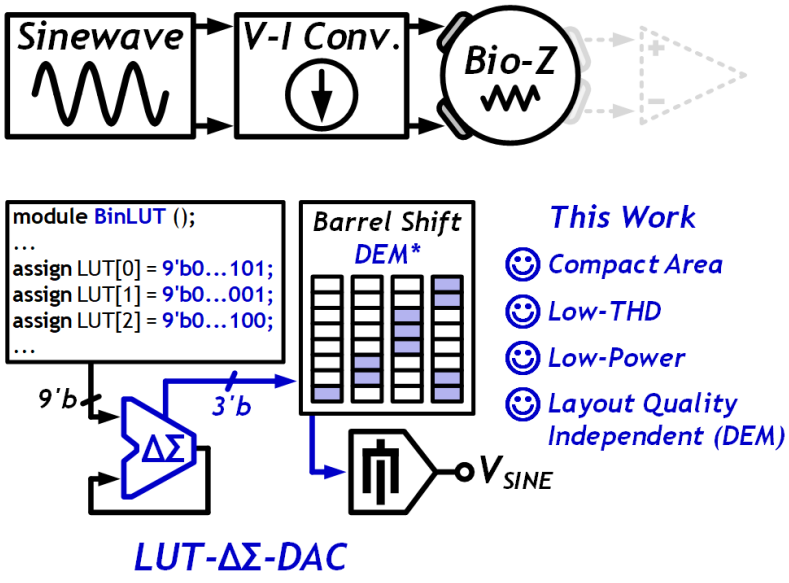

Figure 33. Illustration for the digital part in the proposed sinusoidal CG IC.

4.2.1 Synthesis of the Sinusoid

Figure 34 shows the waveform of integer-numbered sinewave, with the achievable spectrum in frequency domain. In [2], [3] and [30], 6 bit integer-resoludion and 64× sampled sinewave is used. However, its low-frequency spurs exhibited limited spurious-free dynamic range (SFDR) performance of ~47 dBc which eventually makes it impossible to achieve a sub-0.5% THD performance, thus limiting the final accuracy of the Bio-Z sensing. Therefore in this work, we adopted 9 bit quantization step and a 128× sampled pseudo-sine waveform in order to achieve a >60 dBc SFDR performance, which corresponds to a 0.1% of ratio regarding to the fundamental tone. The higher resolution of sinusoid quantization provides significantly improved low-frequency spurs, and the higher rate of sinusoid sampling allows to achieve low-spur near the clock frequency, reducing the overall spur levels down to less than -60 dBc, except for the dominant spur of clock frequency. Note that the dominant spur near the clock frequency still remains as ~42 dBc, however, it can be cleared out by

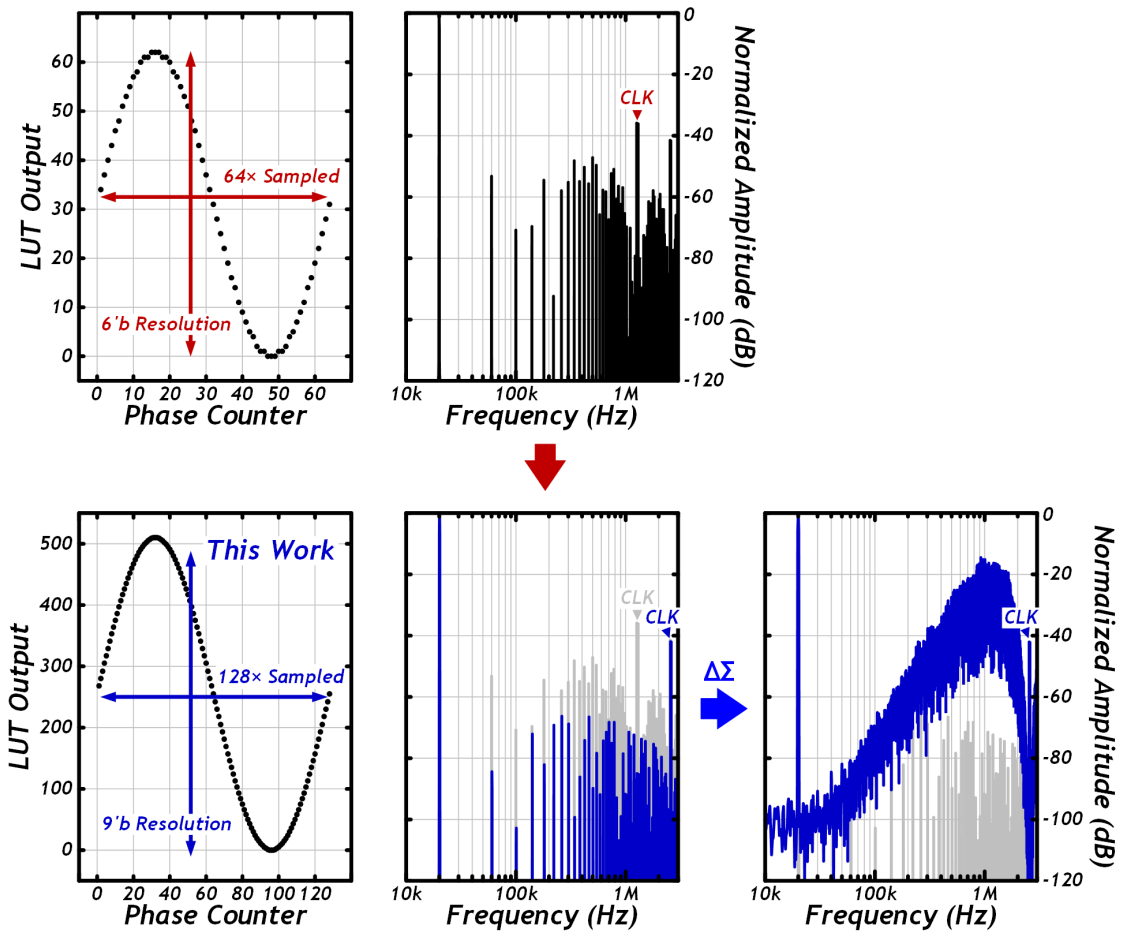

Figure 34. Time-domain and frequency-domain representation of pseudo-sine synthesizer.

the 2nd-order LPF which follows the capacitive-DAC as depicted in Figure 31. In addition, a doubled sampling ratio from 64× to 128× helps to relax the filter design requirements. Finally, when it is 3rd-order ΔΣ modulated, the output spectrum looks like rightmost graph of Figure 34. With the 20 kHz of output frequency, we can expect the overall noise sources, including spurs and quantization noise, can be suppressed down below the -60 dBc, after low-pass filtering.

Alghouth similar concept of this approach was provided in [35], it required a large-bit-width of 18 bit in PRNG to dither its poor spur performance of the oscillator, degrading its power efficiency. Here, the most of spur reduction is obtained only by the 9 bit LUT that is sufficient to provide > 70dB of in-band spur. Furthermore, the use of error-feedback-based ΔΣ modulator halves the required number of accumulators in each of the modulator stages compared to the output-feedback structure [35], greatly simplifying the implementation of the ΔΣ modulator.

The integer-numbered sinewave is generated using MATLAB environment. Detailed MATLAB code is provided as below.

Table II. MATLAB Code Used for the Generation of Pseudo-Sine Waveform

```
%% Start
% Created by Kwantae Kim, 2019
clc;
clear;
close all;

% Global Parameters
clock=2.56*10^6;
OSR=128;

%% PseudoSine Parameters
Am = OSR*2;                 % Define Amplitude for the Integer Components of LUT
                            % This is not a Pk-Pk value
f = clock/OSR;              % Frequency
AmHigh = Am-1;              % Max. Amplitude
AmLow = -Am+1;              % Min. Amplitude

%% Array Generation (Sine, PseudoSine)
t=1/(f*OSR) : 1/(f*OSR) : (1/f);        % x-axis for Time (1 Period)
Sine=AmHigh*sin(2*pi*f*t);              % Sine Generation

PseudoSineValue = zeros(1,OSR);         % Array for PseudoSine Value
PseudoSineValue(1) = AmLow;
for i = 2:1:Am*2
    PseudoSineValue(i) = PseudoSineValue(i-1)+1;
end
```

```
PseudoSine1 = zeros(1,OSR);              % Array for PseudoSine Waveform
for j = 1:1:OSR
      PseudoSine1(j) = PseudoSineValue(1);
      for k = 2:1:length(PseudoSineValue)
            if abs(Sine(j)-PseudoSineValue(k)) < abs(Sine(j)-PseudoSineValue(k-1))
                  PseudoSine1(j) = PseudoSineValue(k);
            end
      end
end

%% Plot
figure(1);
stem(t,PseudoSine1, 'color', 'r');
hold on;
plot(t,Sine,'color','k');

%% Echoing
fprintf('-----Zero Cross Coding-----\n');
fprintf('Frequency = %1.2fkHz\n', (clock/OSR)/1000);

%% Repeating for Spectrum Analyze
% To Widen Frequency Range, Sampling Rate has to be Increased.
% Zero-th Order Hold.
ZOH = 3;
PseudoSine_ZOH = zeros(1,length(PseudoSine1)*ZOH);
for i = 1:1:length(PseudoSine1)
      for j = 1:1:ZOH-1
            PseudoSine_ZOH(ZOH*i-j) = PseudoSine1(i);
      end
      PseudoSine_ZOH(ZOH*i) = PseudoSine1(i);
end

% To Achieve a Fine Resolution BW, # of Samples Should be Increased.
Add_in = 8;
for i = 1:1:Add_in
      PseudoSine_ZOH = [PseudoSine_ZOH PseudoSine_ZOH];
end

%% Plot
figure(2);
sfdr(PseudoSine_ZOH/(AmHigh/sqrt(2)), clock*ZOH);
[SFDR,spurpow,spurfreq] = sfdr(PseudoSine_ZOH, clock*ZOH);
ylim([-80 0])
fprintf('SFDR = %f, at %1.2fMHz (%1.0frd)\n', SFDR, spurfreq/10^6, spurfreq/f);
```

The pseudo-sine signal is approximated to the integer-values in a range of 2^N-2 (in the array of *PseudoSine1* in Table II), where N denotes the resolution of quantization. We ensured that the approximated integer-valued sinewave touches the exact middle point of the full-range (2^N-2) at an integer-multiples of π radian, which helps for the reduction of low-frequency spurs. Because the output of pseudo-sine array is signed-decimal, it is converted into the unsigned-decimal format by adding the maximum value of the array. After it is further converted into the unsigned-binary format, it can be used for the implementation of hardware description language (HDL) in the digital part.

4.2.2 Implementation of the Digital Circuit

Functional verifications of the register transfer level (RTL) design for the digital part of proposed CG IC is done with Cadence Virtuoso (AMS simulator), and the logic synthesis of RTL design is processed with Synopsys Design Compiler.

Table II shows the RTL design of the sinewave synthesizer, using Verilog HDL. Figure 35 describes an instantiation-tree of the RTL design.

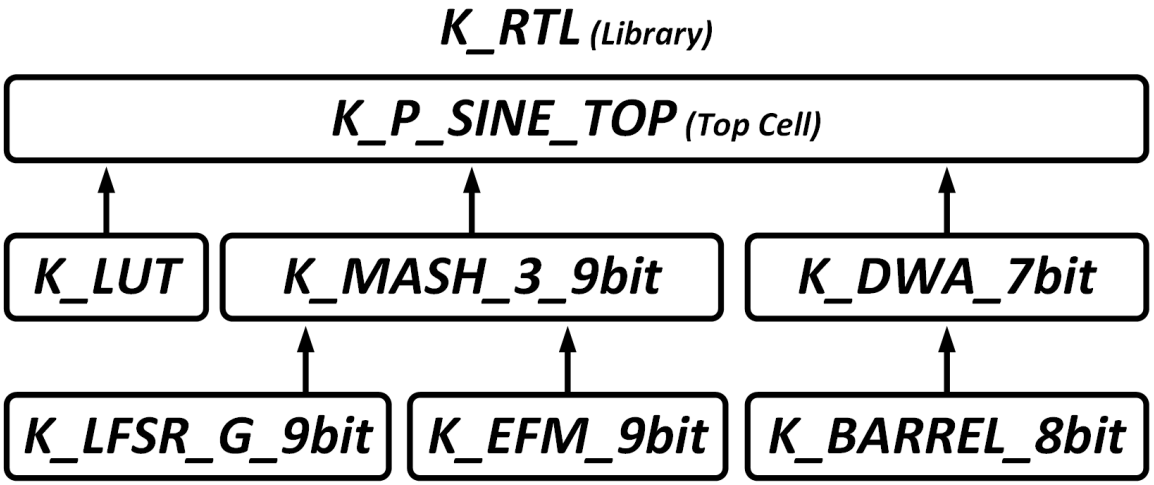

Figure 35. Instantiation-tree of the RTL design.

Table III. Register Transfer Level Design of the Digital Part

```
//Verilog HDL for "K_RTL", "K_P_SINE_TOP" "functional"

module K_P_SINE_TOP (
        input wire      clk,
        input wire      resetn,
        output wire     [7:0] sine_outp,
        output wire     [7:0] sine_outn,
        output wire     sine_dac_rst_p,
        output wire     sine_dac_rst_n
);

wire [8:0] lut_out;
K_LUT
lut(
        .clk    (clk),
        .resetn (resetn),
        .out    (lut_out)
);

wire [6:0] dsm_out;
```

```
K_MASH_3_9bit
dsm(
        .clk    (clk),
        .resetn (resetn),
        .in             (lut_out),
        .out    (dsm_out)
);

K_DWA_7bit
dwa(
        .clk            (clk),
        .resetn         (resetn),
        .in                     (dsm_out),
        .outp           (sine_outp),
        .outn           (sine_outn),
        .dac_rst_p      (sine_dac_rst_p),
        .dac_rst_n      (sine_dac_rst_n)
);

endmodule
```

```
//Verilog HDL for "K_RTL", "K_LUT" "functional"

module K_LUT (
        input wire      clk,
        input wire      resetn,
        output reg      [8:0] out
);

wire [8:0] LUT[127:0];                  // 128 elements of 9bit output
wire [8:0] out_buf;
reg [6:0] counter;                      // 7bit counter for 128 elements
assign out_buf = LUT[counter];          // Combinational logic output

// LUT
assign LUT      [0]     =       9'b     100001100       ;
assign LUT      [1]     =       9'b     100011000       ;
assign LUT      [2]     =       9'b     100100100       ;
assign LUT      [3]     =       9'b     100110001       ;
assign LUT      [4]     =       9'b     100111101       ;
assign LUT      [5]     =       9'b     101001001       ;
assign LUT      [6]     =       9'b     101010101       ;
assign LUT      [7]     =       9'b     101100001       ;
assign LUT      [8]     =       9'b     101101100       ;
assign LUT      [9]     =       9'b     101110111       ;
assign LUT      [10]    =       9'b     110000010       ;
assign LUT      [11]    =       9'b     110001101       ;
assign LUT      [12]    =       9'b     110010111       ;
assign LUT      [13]    =       9'b     110100001       ;
assign LUT      [14]    =       9'b     110101010       ;
assign LUT      [15]    =       9'b     110110011       ;
assign LUT      [16]    =       9'b     110111100       ;
assign LUT      [17]    =       9'b     111000100       ;
assign LUT      [18]    =       9'b     111001100       ;
assign LUT      [19]    =       9'b     111010011       ;
assign LUT      [20]    =       9'b     111011010       ;
assign LUT      [21]    =       9'b     111100000       ;
assign LUT      [22]    =       9'b     111100110       ;
```

```
assign LUT [23] = 9'b 111101011 ;
assign LUT [24] = 9'b 111101111 ;
assign LUT [25] = 9'b 111110011 ;
assign LUT [26] = 9'b 111110110 ;
assign LUT [27] = 9'b 111111001 ;
assign LUT [28] = 9'b 111111011 ;
assign LUT [29] = 9'b 111111101 ;
assign LUT [30] = 9'b 111111110 ;
assign LUT [31] = 9'b 111111110 ;
assign LUT [32] = 9'b 111111110 ;
assign LUT [33] = 9'b 111111101 ;
assign LUT [34] = 9'b 111111011 ;
assign LUT [35] = 9'b 111111001 ;
assign LUT [36] = 9'b 111110110 ;
assign LUT [37] = 9'b 111110011 ;
assign LUT [38] = 9'b 111101111 ;
assign LUT [39] = 9'b 111101011 ;
assign LUT [40] = 9'b 111100110 ;
assign LUT [41] = 9'b 111100000 ;
assign LUT [42] = 9'b 111011010 ;
assign LUT [43] = 9'b 111010011 ;
assign LUT [44] = 9'b 111001100 ;
assign LUT [45] = 9'b 111000100 ;
assign LUT [46] = 9'b 110111100 ;
assign LUT [47] = 9'b 110110011 ;
assign LUT [48] = 9'b 110101010 ;
assign LUT [49] = 9'b 110100001 ;
assign LUT [50] = 9'b 110010111 ;
assign LUT [51] = 9'b 110001101 ;
assign LUT [52] = 9'b 110000010 ;
assign LUT [53] = 9'b 101110111 ;
assign LUT [54] = 9'b 101101100 ;
assign LUT [55] = 9'b 101100001 ;
assign LUT [56] = 9'b 101010101 ;
assign LUT [57] = 9'b 101001001 ;
assign LUT [58] = 9'b 100111101 ;
assign LUT [59] = 9'b 100110001 ;
assign LUT [60] = 9'b 100100100 ;
assign LUT [61] = 9'b 100011000 ;
assign LUT [62] = 9'b 100001100 ;
assign LUT [63] = 9'b 011111111 ;
assign LUT [64] = 9'b 011110010 ;
assign LUT [65] = 9'b 011100110 ;
assign LUT [66] = 9'b 011011010 ;
assign LUT [67] = 9'b 011001101 ;
assign LUT [68] = 9'b 011000001 ;
assign LUT [69] = 9'b 010110101 ;
assign LUT [70] = 9'b 010101001 ;
assign LUT [71] = 9'b 010011101 ;
assign LUT [72] = 9'b 010010010 ;
assign LUT [73] = 9'b 010000111 ;
assign LUT [74] = 9'b 001111100 ;
assign LUT [75] = 9'b 001110001 ;
assign LUT [76] = 9'b 001100111 ;
assign LUT [77] = 9'b 001011101 ;
assign LUT [78] = 9'b 001010100 ;
assign LUT [79] = 9'b 001001011 ;
assign LUT [80] = 9'b 001000010 ;
assign LUT [81] = 9'b 000111010 ;
```

```
assign LUT      [82]    =       9'b     000110010       ;
assign LUT      [83]    =       9'b     000101011       ;
assign LUT      [84]    =       9'b     000100100       ;
assign LUT      [85]    =       9'b     000011110       ;
assign LUT      [86]    =       9'b     000011000       ;
assign LUT      [87]    =       9'b     000010011       ;
assign LUT      [88]    =       9'b     000001111       ;
assign LUT      [89]    =       9'b     000001011       ;
assign LUT      [90]    =       9'b     000001000       ;
assign LUT      [91]    =       9'b     000000101       ;
assign LUT      [92]    =       9'b     000000011       ;
assign LUT      [93]    =       9'b     000000001       ;
assign LUT      [94]    =       9'b     000000000       ;
assign LUT      [95]    =       9'b     000000000       ;
assign LUT      [96]    =       9'b     000000000       ;
assign LUT      [97]    =       9'b     000000001       ;
assign LUT      [98]    =       9'b     000000011       ;
assign LUT      [99]    =       9'b     000000101       ;
assign LUT      [100]   =       9'b     000001000       ;
assign LUT      [101]   =       9'b     000001011       ;
assign LUT      [102]   =       9'b     000001111       ;
assign LUT      [103]   =       9'b     000010011       ;
assign LUT      [104]   =       9'b     000011000       ;
assign LUT      [105]   =       9'b     000011110       ;
assign LUT      [106]   =       9'b     000100100       ;
assign LUT      [107]   =       9'b     000101011       ;
assign LUT      [108]   =       9'b     000110010       ;
assign LUT      [109]   =       9'b     000111010       ;
assign LUT      [110]   =       9'b     001000010       ;
assign LUT      [111]   =       9'b     001001011       ;
assign LUT      [112]   =       9'b     001010100       ;
assign LUT      [113]   =       9'b     001011101       ;
assign LUT      [114]   =       9'b     001100111       ;
assign LUT      [115]   =       9'b     001110001       ;
assign LUT      [116]   =       9'b     001111100       ;
assign LUT      [117]   =       9'b     010000111       ;
assign LUT      [118]   =       9'b     010010010       ;
assign LUT      [119]   =       9'b     010011101       ;
assign LUT      [120]   =       9'b     010101001       ;
assign LUT      [121]   =       9'b     010110101       ;
assign LUT      [122]   =       9'b     011000001       ;
assign LUT      [123]   =       9'b     011001101       ;
assign LUT      [124]   =       9'b     011011010       ;
assign LUT      [125]   =       9'b     011100110       ;
assign LUT      [126]   =       9'b     011110010       ;
assign LUT      [127]   =       9'b     011111111       ;

always @ (posedge clk or negedge resetn)        // Phase accumulator
begin
        if(~resetn)
                counter <= 7'd0;
        else if(counter == 7'd127)
                counter <= 7'd0;
        else
                counter <= counter + 7'd1;
end

always @ (posedge clk or negedge resetn)        // Output register
begin
```

```
        if(~resetn)
                out <= 9'd0;
        else
                out <= out_buf;
end

endmodule
```

```
//Verilog HDL for "K_RTL", "K_MASH_3_9bit" "functional"

module K_MASH_3_9bit (
        input wire      clk,
        input wire      resetn,
        input wire      [8:0] in,
        output wire     [6:0] out       // Thermometer coded output
);

// Accumulators
wire [8:0] acc_fb[0:2];                 // 3 arrays of 9bit accumulator output
wire carry[0:2];                        // 3 arrays of accumulator carry
wire dither;                            // PRNG signal for dithering

K_LFSR_G_9bit
lfsr(
        .clk            (clk),
        .resetn         (resetn),
        .out            (dither)
);
K_EFM_9bit
acc_0(
        .clk            (clk),
        .resetn         (resetn),
        .init           (9'd1),
        .in                     (in),
        .carry          (carry[0]),
        .acc_fb         (acc_fb[0])
);
K_EFM_9bit
acc_1(
        .clk            (clk),
        .resetn         (resetn),
        .init           (9'd0),
        .in                     ( {acc_fb[0][8:1], dither} ),
        .carry          (carry[1]),
        .acc_fb         (acc_fb[1])
);
K_EFM_9bit
acc_2(
        .clk            (clk),
        .resetn         (resetn),
        .init           (9'd0),
        .in                     ( {acc_fb[1][8:1], dither} ),
        .carry          (carry[2]),
        .acc_fb         (acc_fb[2])
);

// Error Cancellation Network
reg carry_d1[0:2];              // 3 arrays of 1 delayed accumulator carry
reg carry_d2[0:2];              // 3 arrays of 2 delayed accumulator carry
reg carry_d3[0:2];              // 3 arrays of 3 delayed accumulator carry
```

```
integer i;
always @ (posedge clk or negedge resetn)
begin
        if(~resetn) begin
                for(i=0; i<3; i=i+1)
                        carry_d1[i] <= 1'd0;
        end
        else begin
                for(i=0; i<3; i=i+1)
                        carry_d1[i] <= carry[i];
        end
end
always @ (posedge clk or negedge resetn)
begin
        if(~resetn) begin
                for(i=0; i<3; i=i+1)
                        carry_d2[i] <= 1'd0;
        end
        else begin
                for(i=0; i<3; i=i+1)
                        carry_d2[i] <= carry_d1[i];
        end
end
always @ (posedge clk or negedge resetn)
begin
        if(~resetn) begin
                for(i=0; i<3; i=i+1)
                        carry_d3[i] <= 1'd0;
        end
        else begin
                for(i=0; i<3; i=i+1)
                        carry_d3[i] <= carry_d2[i];
        end
end

// Output
assign out[0] = carry_d3[0];            // From acc_0
assign out[1] = carry_d2[1];
assign out[2] = ~carry_d3[1];           // From acc_1
assign out[3] = carry_d1[2];
assign out[4] = ~carry_d2[2];
assign out[5] = ~carry_d2[2];
assign out[6] = carry_d3[2];            // From acc_2

endmodule
```

```
//Verilog HDL for "K_RTL", "K_LFSR_G_9bit" "functional"

module K_LFSR_G_9bit (
        input wire clk,
        input wire resetn,
        output reg out
);

// Target: x9+x5+1
reg [8:0] shift_reg;            // 9bit LFSR
wire xor_out;
assign xor_out = shift_reg[3] ^ shift_reg[8];
```

```
always @ (posedge clk or negedge resetn)
begin
        if(~resetn)
                shift_reg <= 9'd1;  // Non-zero initial condition
        else
                shift_reg <= {shift_reg[7:4], xor_out, shift_reg[2:0], shift_reg[8]};
end

always @ (posedge clk or negedge resetn)
begin
        if(~resetn)
                out <= 1'd0;
        else
                out <= shift_reg[8];
end

endmodule
```

```
//Verilog HDL for "K_RTL", "K_EFM_9bit" "functional"

module K_EFM_9bit(
        input wire              clk,
        input wire              resetn,
        input wire              [8:0] init,     // 9bit initial condition
        input wire              [8:0] in,       // 9bit input
        output wire             carry,          // DSM output
        output reg              [8:0] acc_fb    // 9bit error feedback
);

wire [9:0] acc_total;                           // 10bit accumulator output
assign acc_total = {1'd0, in} + {1'd0, acc_fb};
assign carry = acc_total[9];

always @ (posedge clk or negedge resetn)
begin
        if(~resetn)
                acc_fb <= init;
        else
                acc_fb <= acc_total[8:0];
end

endmodule
```

```
//Verilog HDL for "K_RTL", "K_DWA_7bit" "functional"

module K_DWA_7bit (
        input wire      clk,
        input wire      resetn,
        input wire      [6:0] in,       // 7bit thermometer coded input
        output reg      [7:0] outp,     // 8bit thermometer coded output
        output reg      [7:0] outn,
        output reg      dac_rst_p,
        output reg      dac_rst_n
);

// Input realignment
wire    [2:0] in_buf_B;
assign  in_buf_B = {2'd0, in[6]}
                + {2'd0, in[5]}
                + {2'd0, in[4]}
                + {2'd0, in[3]}
```

```
                    + {2'd0, in[2]}
                    + {2'd0, in[1]}
                    + {2'd0, in[0]};                                    // Thermometer to binary

wire        [6:0] in_buf_T;
assign      in_buf_T = (in_buf_B == 3'd0) ? 7'b000_0000 :
                       (in_buf_B == 3'd1) ? 7'b100_0000  :
                       (in_buf_B == 3'd2) ? 7'b110_0000  :
                       (in_buf_B == 3'd3) ? 7'b111_0000  :
                       (in_buf_B == 3'd4) ? 7'b111_1000  :
                       (in_buf_B == 3'd5) ? 7'b111_1100  :
                       (in_buf_B == 3'd6) ? 7'b111_1110  :
                                            7'b111_1111;                // Binary to thermometer

// Pointer
reg         [3:0] pnt;              // 4bit pointer
always @ (posedge clk or negedge resetn)
begin
            if(~resetn)
                        pnt <= 4'd0;
            else
                        pnt <= ( pnt + {1'd0, in_buf_B} ) % (4'd8);
end

// Barrel Shift
wire        [7:0] out_buf;      // 8bit thermometer coded output buffer
K_BARREL_8bit
barrel_sft(
            .in                 ( {in_buf_T, 1'd0} ),
            .sft        (pnt[2:0]),
            .out        (out_buf)
);

// Output
always @ (posedge clk or negedge resetn)
begin
            if(~resetn)
                        outp <= 8'd0;
            else
                        outp <= out_buf;
end
always @ (posedge clk or negedge resetn)
begin
            if(~resetn)
                        outn <= 8'd0;
            else
                        outn <= ~out_buf;
end
always @ (posedge clk or negedge resetn)
begin
            if(~resetn)
                        dac_rst_p <= 1'd1;
            else begin
                        if (in_buf_B == 3'd0)
                                    dac_rst_p <= 1'd1;
                        else
                                    dac_rst_p <= 1'd0;
            end
end
```

```
always @ (posedge clk or negedge resetn)
begin
        if(~resetn)
                dac_rst_n <= 1'd1;
        else begin
                if(in_buf_B == 3'd7)
                        dac_rst_n <= 1'd1;
                else
                        dac_rst_n <= 1'd0;
        end
end

endmodule
```

```
//Verilog HDL for "K_RTL", "K_BARREL_8bit" "functional"

module K_BARREL_8bit(
        input wire      [7:0] in,       // 8bit thermometer coded input
        input wire      [2:0] sft,
        output wire     [7:0] out       // 8bit thermometer coded output
);

wire [15:0] in_buf;                     // 16bit input buffer
wire [15:0] out_buf;                    // 16bit output buffer

assign in_buf = {in, in};
assign out_buf = in_buf >> sft;
assign out = out_buf[7:0];

endmodule
```

In the implementation of pseudo-sine LUT (K_LUT in Table III), bit-width of the phase accumulator (or phase counter) is implemented as a 7 bit which corresponds to 128× sampled sinusoidal waveform. For the design of ΔΣ modulator (*K_MASH_3_9bit* in Table III), we applied odd numbered initial condition (9'd1) to the 1st-accumulator to reduce periodic-pattern-induced spurs which is intrinsic behavior of the digital ΔΣ modulator [55].

The implemented PRNG dithers the input LSB of 2nd and 3rd-accumulators which results in a noise-shaped random noise addition [56], to further reduce the spurs. This PRNG (*K_LFSR_G_9bit* in Table III) is designed using Galois linear-feedback shift register (LFSR) architecture, which is also called as maximum length sequence (MLS), and it is more hardware-efficient design compared to its Fibonacci LFSR counterpart [35]. This is because the Galois LFSR architecture has less combinational logic delay, as there are no multiple serialized XOR gate connections existing. Note that the initial condition of the shift register in LFSR is non-zero, because of its ring-connected structure.

The DWA block (*K_DWA_7bit* in Table III) helps to enhance the linearity of the DAC by noise-

shaped dynamic element matching (DEM) of the DAC unit elements, thus it eliminates layout-dependent linearity degradation and it is amenable to be fully integrated in the standard auto place-and-route (PnR) process without severe performance loss.

4.3 Design of the Analog Current Converter

4.3.1 Capacitive Voltage DAC

The DAC included in the analog part of the proposed CG IC is implemented using the custom-layout metal-oxide-metal (MOM) unit capacitors [57] in a differential manner to achieve a low-power and even harmonic rejection. Since the capacitors are inherently AC-coupled interface, we need anyhow to define the DC-level of the DAC output. For this purpose, a reset switch (SW) is implemented to define the output DC-level of capacitor DAC as a GND potential, where the dummy SW suppresses charge injection and clock-feedthrough, operating in an opposite polarity as shown in Figure 31. When the the output of 3 bit ΔΣ modulated sinewave reaches '000' (also shown shown in *K_DWA_7bit* in Table III), the DAC is reset to the GND using the reset SW.

However, there are some concerns regarding this reset operation using the SW, shown in Figure 36. First, we face a level-dependent glitches when the DAC output make a transition. Second, when the SW is OFF from the ON state, a DC error occurs at the DAC output, such as charge injection and clock-feedthrough. Third, since the reset operation can be viewed as a sampling process which is similar to the case of discrete-time ΔΣ ADC or successive approximation register (SAR) ADC, these non-ideal errors are aliased after the sampling. Fourth, unfortunately, these errors can not be cancelled out through the differential operation, because the reset instant is unequal in differential digital signal. The consideration of these errors are especially important because

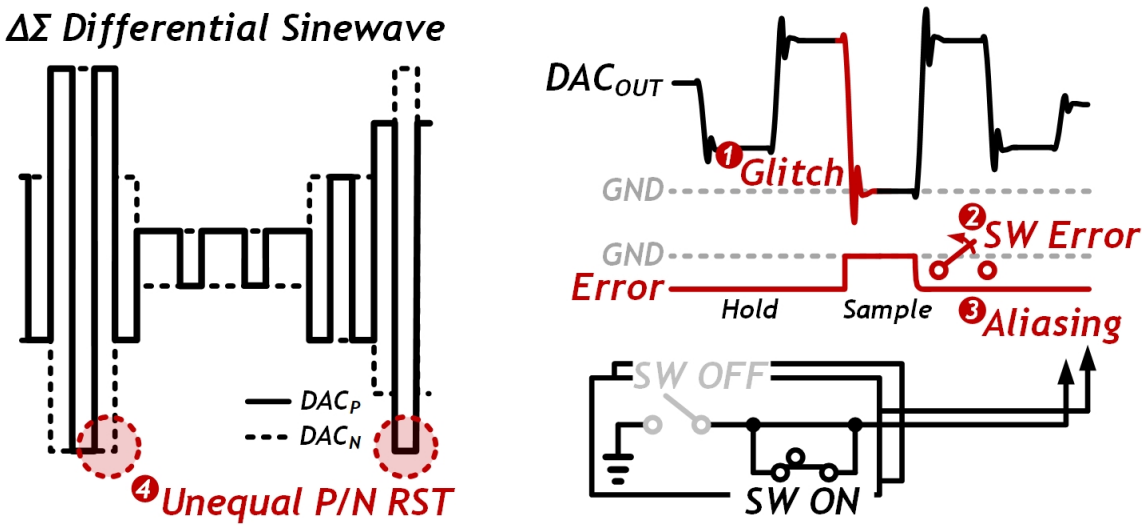

Figure 36. Design issues in the implementation of reset SW.

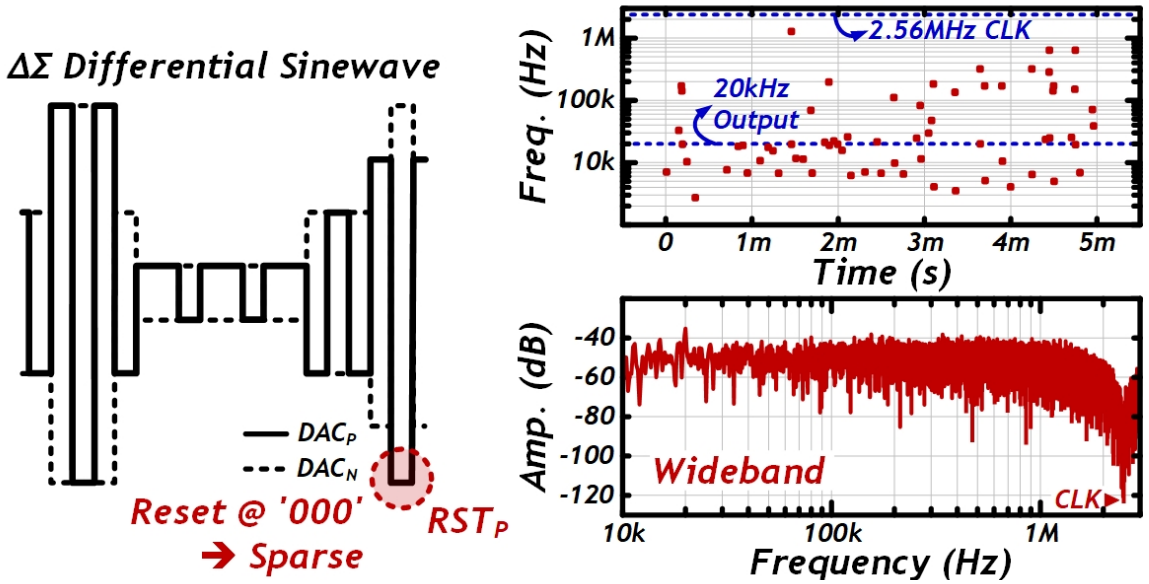

Figure 37. Sparse pattern of the reset signal of the DAC.

the 3 bit ΔΣ modulated sinewave data sparsely reaches '000', thus the frequency of reset operation is relatively low.

Figure 37 shows the frequency and the spectrum of the reset signal. The reset operation is sparse, and more importanatly, this sparse reset operation has no fixed periodic pattern, rather, it is random-number-like wideband signal. As a result, due to the low-frequency sampling process of reset operation, the output spectrum of the DAC shows a large increase of noise floor (Figure 39).

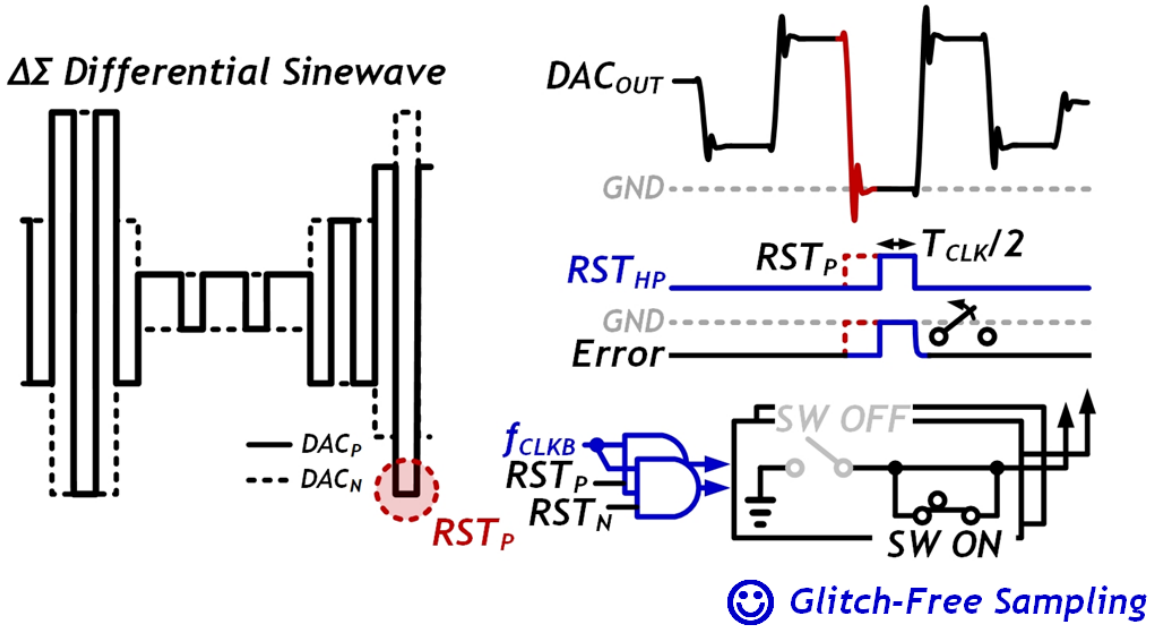

Figure 38. Half-period reset scheme.

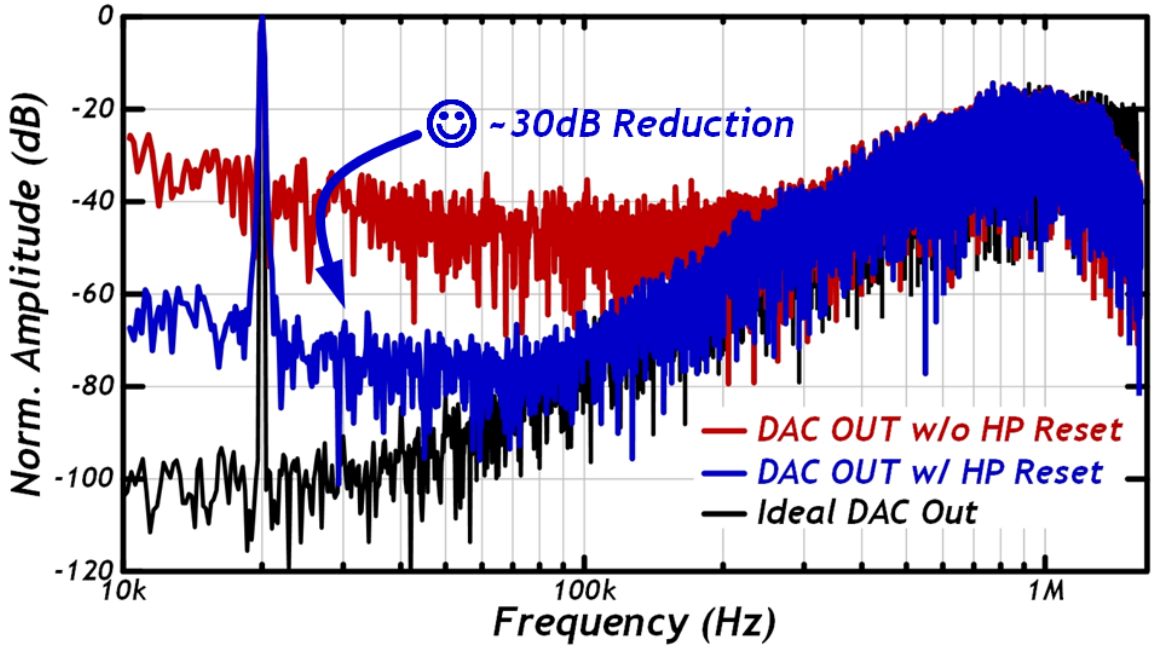

Figure 39. Post-layout simulation result of the half-period reset scheme.

To mitigate this increase of the noise floor, in this work, we propose the use of half-period reset. As shown in Figure 38, when we generate the reset signal using the inverted clock signal and also utilizing AND gates, a reset operation, but with a duration of half-period is provided. Since the half-period reset scheme allows that the reset SW can not be turned ON when the settling behavior due to the switching transient is occurring, glitch-free sampling operation is possible.

As shown Figure 39, the post-layout simulation result shows that a significant increase of in-band noise floor of the DAC output can be avoided about 30 dB with the help of half-period reset scheme. This is sufficient amount to achieve a less than -60 dBc of noise floor, leading to a low-THD performance of the entire sinusoidal CG IC. Note that all of the simulation setup in Figure 39 adopted dummy SW to deal with the non-idealities by a first-order.

Figure 40 shows the implementation of reset SW. Since the leakage current also contributes to the increase of low-frequency noise floor, two design methods are adopted. First, the I/O device is utilized for the main SW part. Second, bootstrapping technique is utilized to drive the gate voltage of reset SW by $\pm V_{DD}$. To maximize the area-efficiency, MOM capacitors are also used here for bootstrapping capacitors, and it is laid out on top of the SW transistors.

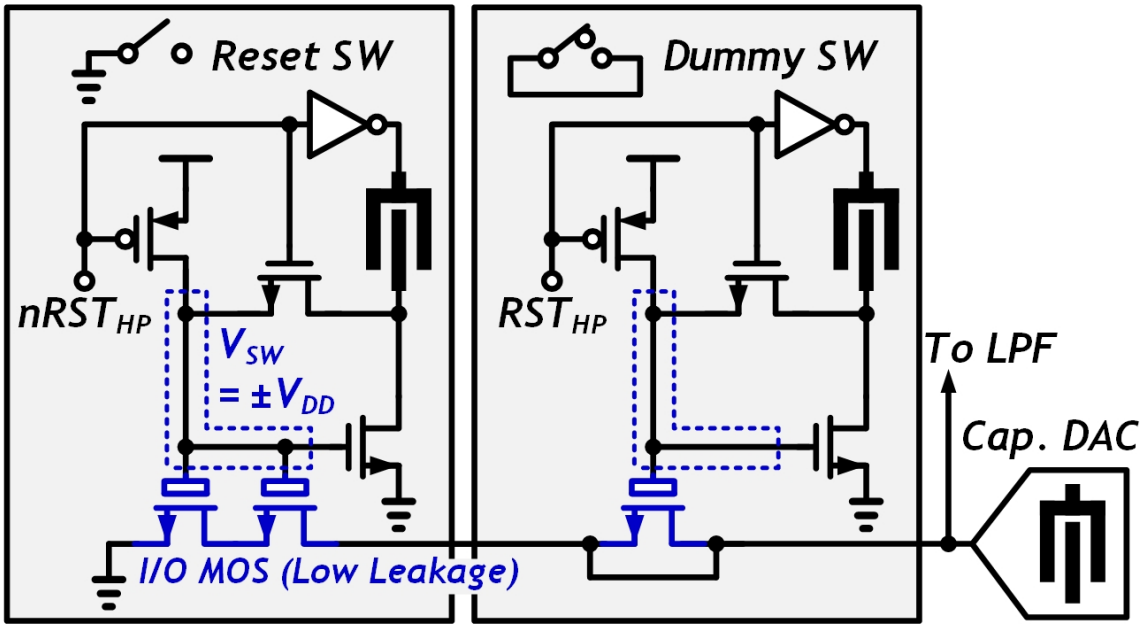

Figure 40. Implementation of bootstrapped SW.

4.3.2 2nd-Order LPF

There are two popular structures for the implementation of post-filtering LPF, one is active-RC filter and the other one is g_m-C filter. In general, active-RC filter has a superiror noise and distortion performance over its g_m-C counterpart. However, the OTA included in the active-RC filter should drive the passive resistor used for RC time constant generation, resulting in a increased power burden. Furthermore, it also necessitates analog voltage buffer because the incoming signal is provided by capacitive DAC as discussed above. On the other hand, as the g_m-C filter has MOSFET-gate input, it obviates the need for the power-consuming analog voltage buffer, nor requiring any of resistive driving from the OTA. Therefore in this design, a source-follower-based 2nd-order g_m-C biquad LPF is adopted.

Figure 41 shows the schematic of LPF [31]. This structure features a simple architecture, an easy tuning capability, and also a low-distortion which is inherent behavior of the source-follower. To lower the harmonic components of the LPF, all of devices are designed to have sufficiently long-channel-length (4 μm in this design), and the V_{DS} of top current sources are ensured to have >150 mV over the PVT corners. Total power consumption of this LPF is designed to have <100 nW.

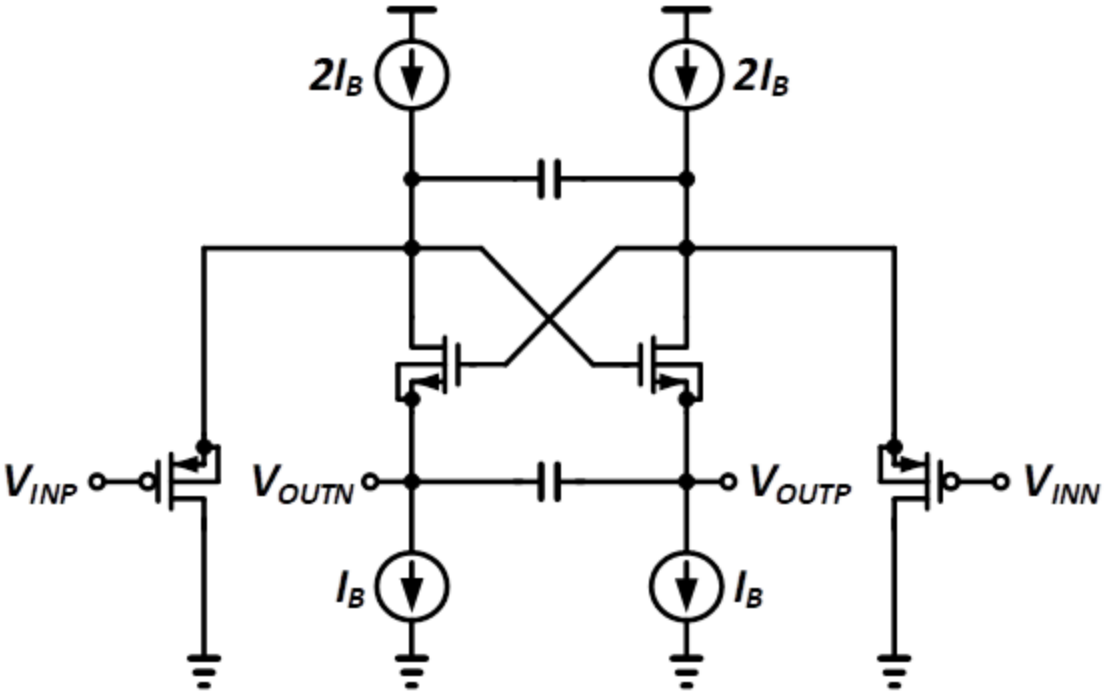

Figure 41. 0.5 V 2nd-order LPF.

4.3.3 V-I Converter

The implemented V-I converter is based on the instrumentation amplifier architecture that includes wide-BW lead-compensated TC stage, as discussed in Chapter 3.1 [29], [30]. It consists of the TC stage which converts the input voltage into the current signal using R_{VI}, and the output stage which is interfacing with the electrodes for the Bio-Z sensing as shown in Figure 42. Instead of providing most of the current consumption at the TC stage, to maximize current efficiency of the V-I converter, 20× larger bias current is designed at the output stage of V-I converter. Furthermore, because there's no need for demodulation choppers, low-side cascode transistors are removed and the headroom condition is more relaxed.

Benefiting from not only wide-BW of lead-compensation but also gain-boosting of the TC stage, this V-I converter achieves 800 kHz BW, >65 dBc SFDR up to 80 kHz of input frequency while consuming only 4.38 μW that is sufficient for our target performance of >60 dBc of linearity.

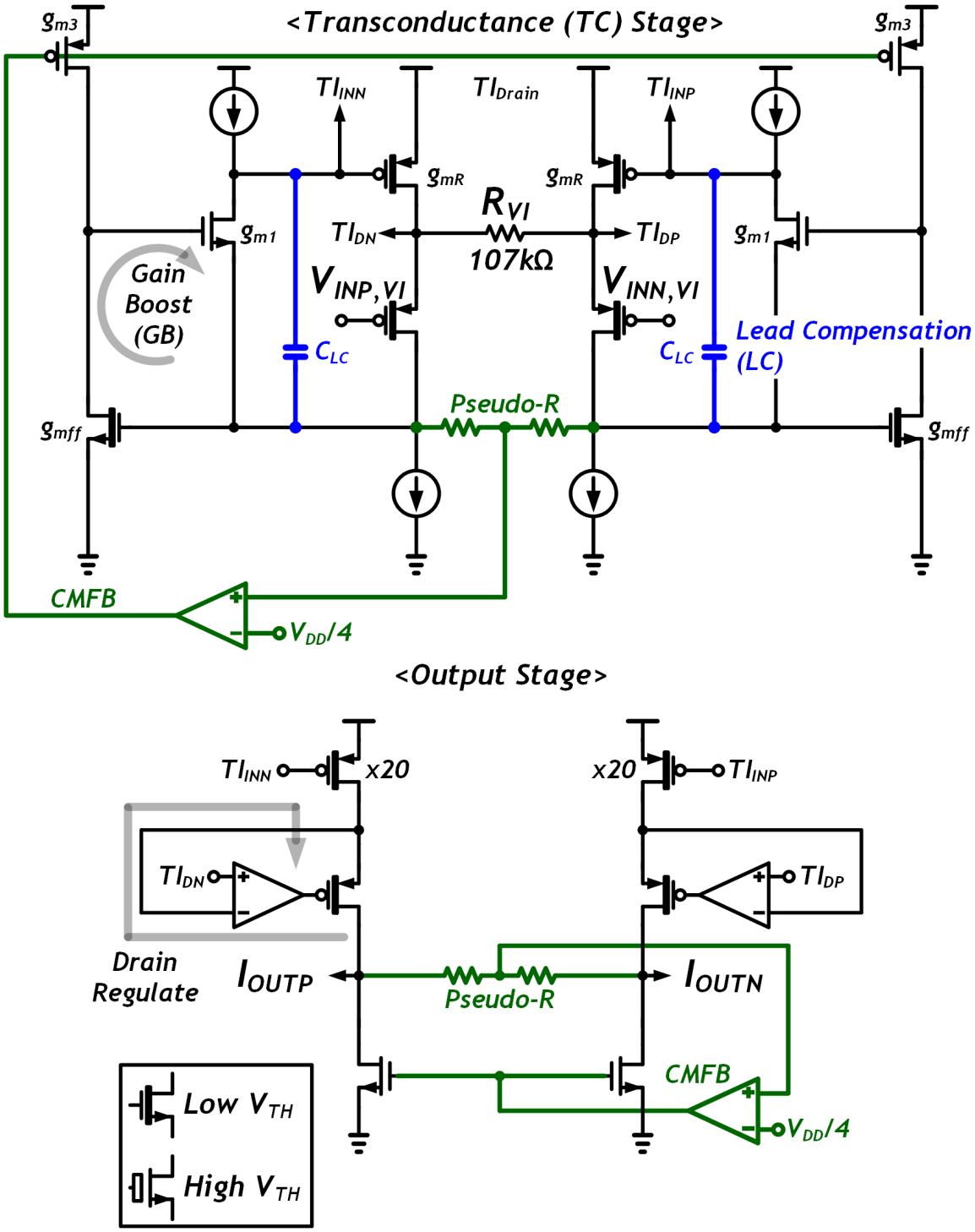

Figure 42. 0.5 V V-I converter based on lead-compensated TC stage.

4.4 Implementation Results

The proposed sinusoidal CG IC is fabricated in a 65 nm CMOS process with a compact area of 0.059 mm^2 (see Figure 43), a low-power of 6.2 µW, and a low-distortion of 0.088% THD. Its digital core has a gate count of 1127 and it is synthesized from the standard auto place-and-route flow. The right-side photograph in Figure 43 shows a closed-up photograph for the CG block, without top 3 metals layers.

To decouple the substrate noise from the digital circuits to the noise-sensitive analog circuits, double guard-ring is utilized as shown in Figure 44. By surrounding the synthesized digital core with the NMOS decap, forming a substrate guard-ring, and further adding one more n-well guard ring, switching noise of the digital circuit through the substrate is minimized. Guard-rings are laid out manually, in the Cadence Virtuoso environment.

Figure 45 shows the the measurement setup. In the proposed CG IC, we designed two versions of our building blocks, one is all blocks are included version which has full signal chain of sinusoidal CG IC, the other one is test version which includes digital core and capacitor-DAC, to measure the output spectrum of the DAC only. The output of the sinusoidal current is driven to the known-valued test resistor, while the output of the capacitor-DAC is buffered using the on-chip source followers. Both of the them are post-amplified, and differential-to-singled-ended converted before they are measured by the oscilloscope. In addition, we also

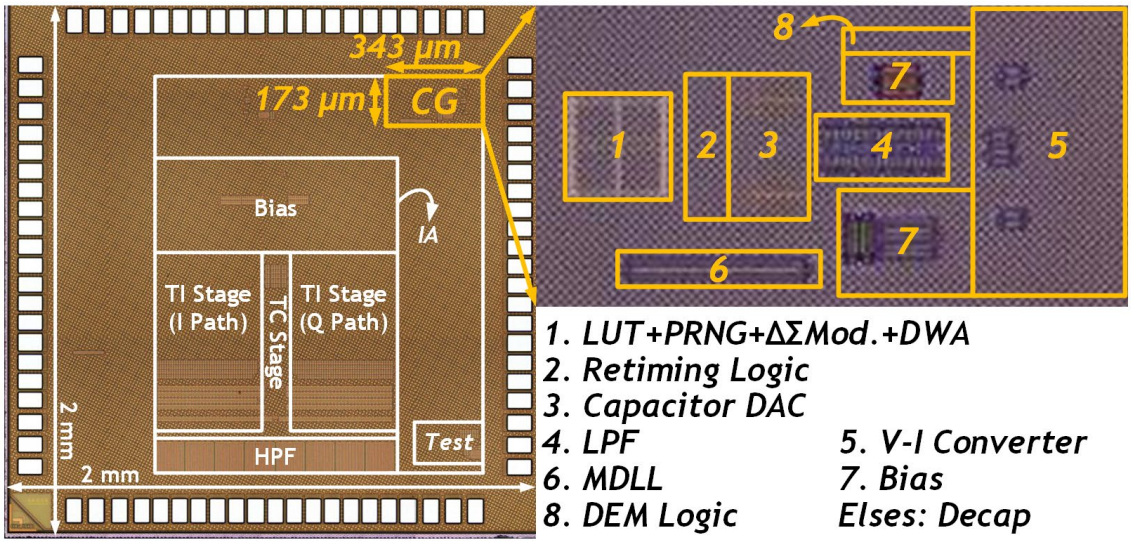

Figure 43. Chip micrograph of the proposed CG IC.

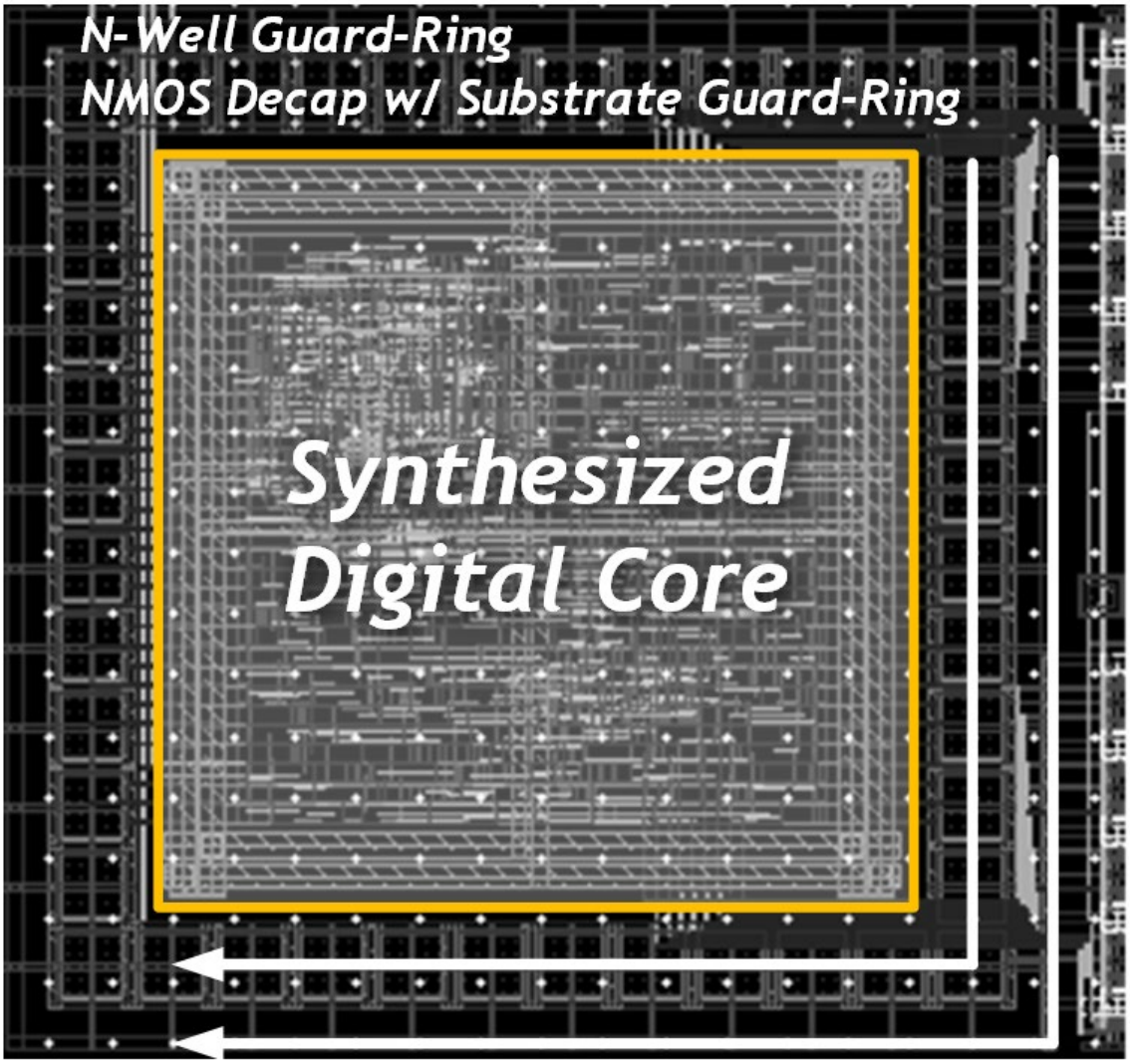

Figure 44. Double guard ring scheme applied to the digital core.

separated the analog supply and the digital supply, to decouple the switching noise coming from the digital circuits and the noise-sensitive analog circuits as much as possible.

Figure 46 shows the measurement result of output spectrum for the full signal chain version of the CG IC in the blue color, while only digital core and DAC version in the black color. The load impedance of the CG IC is set to 970 Ω. It is clearly seen that the DAC output waveform has a 3rd-order noise-shaped spectrum with a 60 dB/dec slope. The output frequency of sinewave is 20kHz. The SFDR performance are measured by 65.17 dBc for the 3rd harmonic of the sinusoidal CG IC, which translates to a 0.088% of the THD performance counting up to 20^{th} harmonics, while the in-band SFDR of 73.8 dBc for the DAC output only. This SFDR performance is mainly bounded by the swing range of the LPF, which has 10 mV_{pp} of the output swing, because

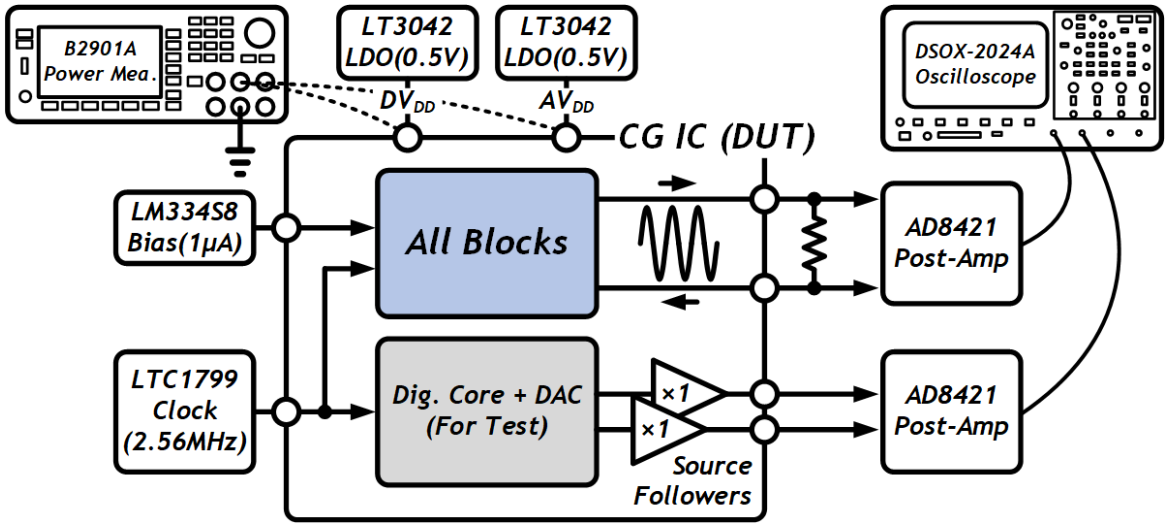

Figure 45. Measurement setup of the proposed CG IC.

of a 0.5V of low-supply. We can also see that 3rd-order noise-shaped quantization noise can not be removed perfectly, because of the limited order of the LPF, which is 2nd-order. All of these performance limits can be improved with the cost of more power consumption, and area occupation of the LPF.

Figure 47 shows the power consumption of the digital core. The digital core has a nominal operating condition of a 2.56 MHz clock frequency and a 0.5 V supply voltage. It consumes only a 1.29 μW, with the help

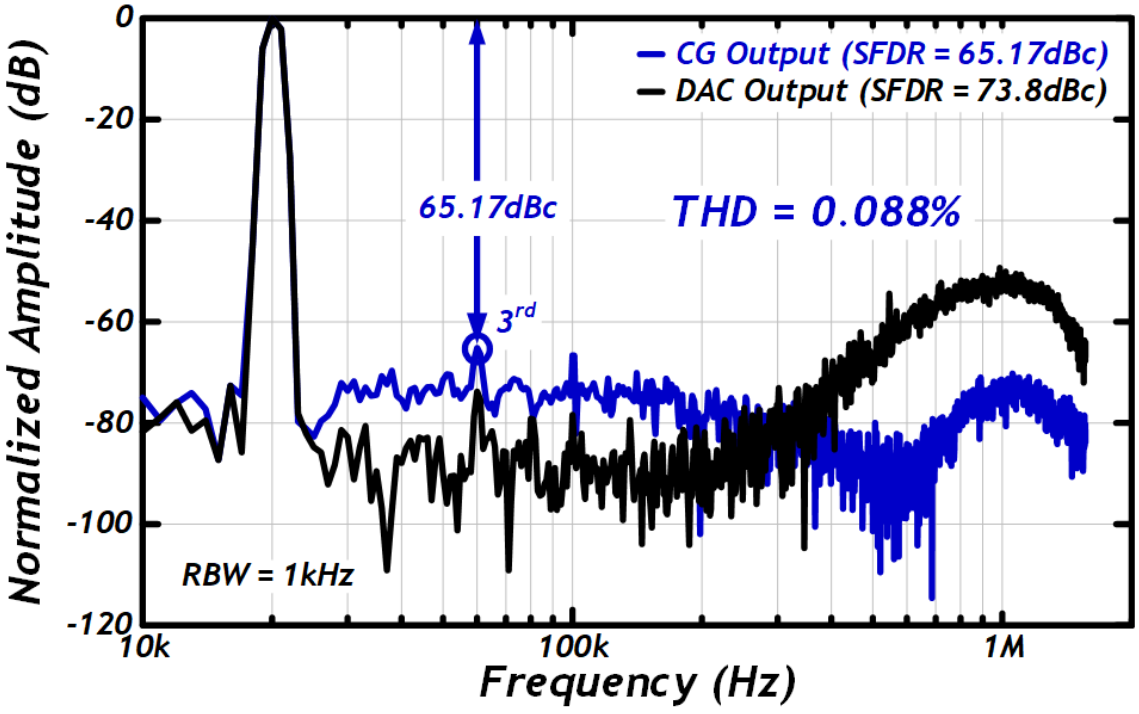

Figure 46. Measured spectrum of the CG and the DAC output.

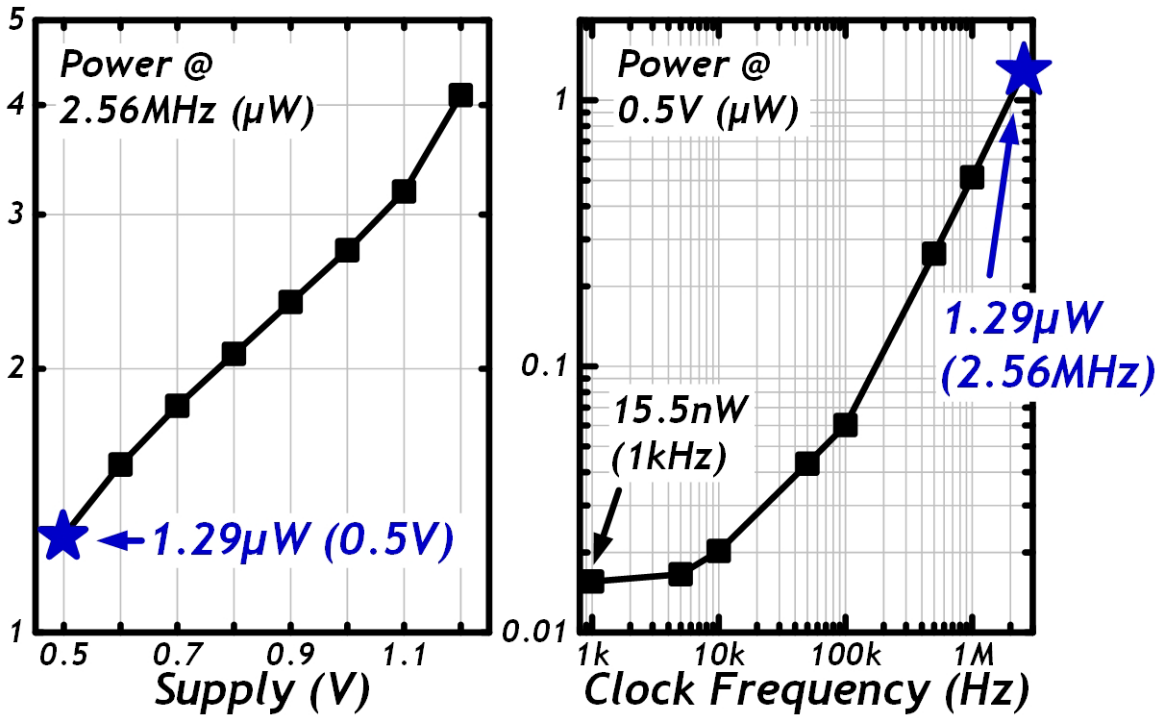

Figure 47. Measured logic power of the digital core.

of near-threshold operation as shown in left-side of figure 47. When the clock frequency of the digital core decreases down to 1 kHz, the power consumption is measured by 15.5 nW and it also indicates the amount of leakage power consumption.

The measured load sensitivity is shown in Figure 48. With a 2 μA_{PP} and a 20 kHz output current, it

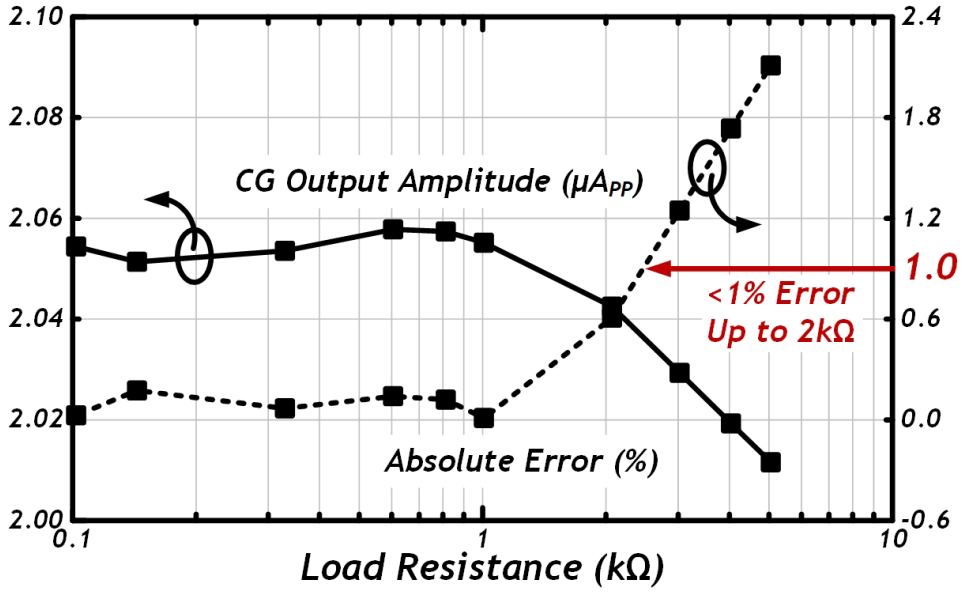

Figure 48. Measured load range the CG.

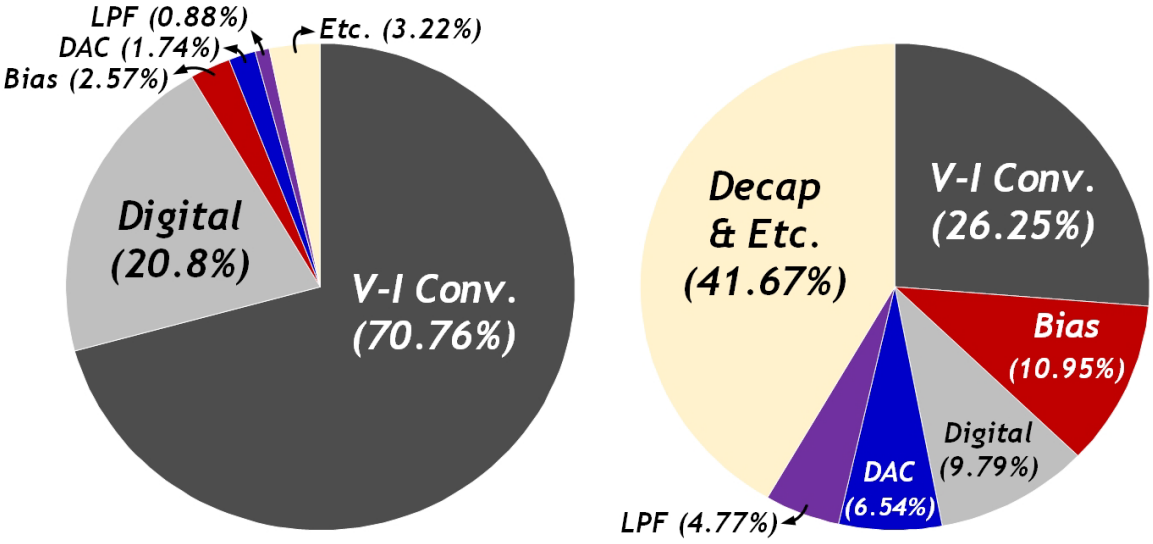

Figure 49. Power and area breakdown of the CG IC.

can drive the load impedance up to 2 kΩ, with less than a 1% of driving error. It is sufficient driving capability for the most of tetra-polar electrode configuration of the Bio-Z monitoring environment.

Figure 49 shows the power and area breakdown of the proposed CG IC. Thanks to the near-threshold operation, the digital circuit contributes to a only 20% of the total power consumption. The most of power consumption is focused on the V-I converter, maximizing the power efficiency of the output current driving. Since the most power-consuming block in the Bio-Z sensor is CG, especially V-I converter [20], [30], it indicates an optimized power distribution is conducted for the ultra-low-power Bio-Z sensor ICs. For the area perspective, most of the area is occupied by the decap and etc., indicating that there is even more room to optimize the area of this work, for example, utilizing fully-synthesizable mixed-signal implementation techniques [52]-[54].

Table IV summarizes the comparison of performances with the previous CG ICs for the Bio-Z sensing applications. The proposed sinusoidal CG IC outperforms previous low-power design [29], [30] by 33× in chip area and by 7.5× in THD. Furthermore, it also outperforms previous low-distortion design [35] by 8.9× in total power and by 1.9× in THD, recording the state-of-the-art low-power, low-distortion, and low-area sinusoidal CG IC for the Bio-Z sensing applications.

Table IV. Performance Summary and Comparison of the CG IC

Comparison	TBioCAS 13 L. Yan	JSSC 15 S. Hong	JSSC 17 M. Kim	TCAS-II 19 S.-K. Hong	ISSCC 19 K. Kim	*This work*
Process (nm)	180	180	65	180	65	65
Supply (V)	1.8	1.8	1.2	-	0.5	***0.5***
Architecture	LUT	RC OSC	LUT	RDO+DT FIR	LUT	LUT+CT LPF
Frequency (kHz)	20	100	128	20	20	20
THD (%)	<1[a]	<0.2	<0.5	0.17	0.66	***0.088***
Load Range (kΩ)	4.4	1	100	1	-	2
Inj. Current (μA_{pp})	40	200	100	40	8.4	2
Total Power (μW)	54	-	-	55.6	5.31	***6.2***
Area (mm^2)	0.74[b]	0.91	0.37[b]	0.052	1.958	***0.059***

[a] THD after demodulation [b] Estimated from chip photo

Chapter 5. Conclusion

It this dissertation paper, two dedicated application-specific integrated circuit (ASIC) are developed with 65 nm CMOS technology. Both chips are targetted for the ultra-low-power continuous Bio-Z sensing system (e.g. cardiac pacemaker).

The first chip is a 0.5 V lowest supply Bio-Z sensor IC ever reported, achieving a 9.26 μW of power consumption and a 0.57º of phase error performance under 10% of supply and 0ºC-70ºC of temperature variations using a 20 kHz modulation frequency. Together with its 2% of magnitude error and 0.4º of phase error in the range of 126 Ω magnitude and 3º-8º phase range, the continuous fluid status monitoring of the CHF patients can be possible; 200 $m\Omega_{PP}$ of the TIV detection is shown by an experimental test on the human body, benefiting from its 15.28 mΩ/√Hz low-noise performance. For the low-supply operation, the dedicated current-feedback IA and LDO-based V–I converters are proposed. Especially, the auxiliary LDO is proposed to reject $I_{Residue}$ within the V–I converter, which allows an 8.4 μA_{PP} sinusoidal current injection consuming only a 4.62 μW power with a 0.66% THD. For the low phase error, the IA features the lead-compensated TC stage that exhibits a wide BW of a 408 kHz but consuming only a 3.95 μW, which is 11.65× and 3.19× improvement over the recently published IA design, respectively.

The second chip is the first sub-10 μW (6.2 μW) of power and sub-0.1% (0.088%) of THD sinusoidal CG IC operating under a 0.5 V low-supply with 20 kHz modulation frequency. The implemented digital core has gate count of 1127 which is operating from 2.56 MHz, consuming only a 1.29 μW of power consumption and resulting in a compact area of 0.059 mm^2. The utilization of digital ΔΣ modulation applied to the sinewave LUT leads to a low bit (3 bit) DAC and a compact area. Not only to use the power-efficient MOM capacitor DAC, but also to achieve a low noise floor, the half-period reset scheme is proposed. The three key specifications of the proposed CG IC outperforms state-of-the-art designs by 33× in chip area, by 7.5× in THD, and by 8.9× in total power respectively.

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Curriculum Vitae

Kwantae Kim

Personal

Bio-Medical Sensor IC Design

IEEE ISSCC 2019 ***IEEE JSSC 2020***

► Developed a low-phase (φ) error and low-power bio-impedance (Bio-Z) sensor IC for long-term monitoring of cardiac patients

IEEE VLSI Symposium 2020

► Developed a low-distortion and low-power sinusoidal current generator IC for Bio-Z sensors

Participated in the design of 10 Silicon Chips of deep sub-micron CMOS circuits over 5 years

► 3 chips with ***180nm*** (SMIC, TSMC) and 6 chips with ***65nm*** (Samsung, TSMC)

Education

Visiting Student **in Institute of Neuroinformatics, Univ. of Zurich/ETH Zurich** **Feb.-Sep. 2020**

Ph.D. Student **in Electrical Engineering, KAIST** (KAIST Scholarship) **Feb. 2021**

M.S. **in Electrical Engineering, KAIST** **Feb. 2017**

► Thesis title: Low-Power Fast-Settling Bio-Impedance Sensor for Portable Pressure Monitor

B.S. **in Electrical Engineering, KAIST** (National Scholarship) **Feb. 2015**

Summer Session **in Mathematics, Univ. of California, Berkeley** **Jun.-Aug. 2013**

Work Experience

Healthrian Co., Ltd. (Full-Time Employment) **2015-2017**

► In-vivo measurement and data collection of wrist Bio-Z for watch-type blood pressure monitoring system

Awards

IDEC Congress Chip Design Contest (CDC) (Best Poster Award) **Jun. 2019**

25th Samsung Humantech Paper Award (Silver Prize, as a Leading Author) **Feb. 2019**

KAIST-Keio-Tsinghua (KKT) Workshop (Best Paper in Poster Session) **Aug. 2015**

Un Chong-Kwan Scholarship Award (1st Place in Entrance Examination) **Apr. 2015**

Publications (Leading Author)

Journals

IEEE JSSC 2020

A 0.5 V Sub-10 µW 15.28 mΩ/√Hz Bio-Impedance Sensor IC with Sub-1º Phase Error

► ***Kwantae Kim***, Ji-Hoon Kim, Surin Gweon, Minseo Kim, and Hoi-Jun Yoo

JSTS 2017

A 55.77 µW Bio-impedance Sensor with 276 µs Settling Time for Portable Blood Pressure Monitoring System

► ***Kwantae Kim***, Minseo Kim, Hyunwoo Cho, Kwonjoon Lee, and Hoi-Jun Yoo

Conferences

IEEE VLSI Symposium 2020

A 0.5V, 6.2µW, 0.059mm^2 Sinusoidal Current Generator IC with 0.088% THD for Bio-Impedance Sensing

► ***Kwantae Kim,*** Changhyeon Kim, Sungpill Choi, and Hoi-Jun Yoo

IEEE ISSCC 2019

A 0.5V 9.26µW 15.28mΩ/√Hz Bio-Impedance Sensor IC with 0.55º Overall Phase Error

► ***Kwantae Kim,*** Ji-Hoon Kim, Surin Gweon, Jiwon Lee, Minseo Kim, Yongsu Lee, Soyeon Kim, and Hoi-Jun Yoo

IEEE ESSCIRC 2017

A 24 µW 38.51 mΩ_{rms} Resolution Bio-Impedance Sensor with Dual Path Instrumentation Amplifier

► ***Kwantae Kim,*** Kiseok Song, Kyeongryeol Bong, Jaehyuk Lee, Kwonjoon Lee, Yongsu Lee, Unsoo Ha, and Hoi-Jun Yoo

IEEE ISCAS 2016

A 54-µW Fast-Settling Arterial Pulse Wave Sensor for Wrist Watch Type System

► ***Kwantae Kim,*** Minseo Kim, Hyunwoo Cho, Kwonjoon Lee, Seung-Tak Ryu, and Hoi-Jun Yoo

Publications (Co-Author)

Journals

IEEE JSSC 2017

A 1.4-mΩ-Sensitivity 94-dB Dynamic-Range Electrical Impedance Tomography SoC and 48-Channel Hub-SoC for 3-D Lung Ventilation Monitoring System

► Minseo Kim, Minseo Kim, Jaeeun Jang, Hyunki Kim, Jihee Lee, Jaehyuk Lee, Jiwon Lee, Kyoung-Rog Lee, ***Kwantae Kim,*** Yongsu Lee, Kyuho Jason Lee, and Hoi-Jun Yoo

Conferences

IEEE CICC 2020

A 9.6 mW/Ch 10 MHz Wide-bandwidth Electrical Impedance Tomography IC with Accurate Phase Compensation for Breast Cancer Detection

► Jaehyuk Lee, Surin Gweon, Kwonjoon Lee, Soyeon Um, Kyoung-Rog Lee, ***Kwantae Kim,*** Jihee Lee, and Hoi-Jun Yoo

IEEE ISCAS 2019

93.8% Current Efficiency and 0.672 ns Transient Response Reconfigurable LDO for Wireless Sensor Network Systems

► Surin Gweon, Jaehyuk Lee, ***Kwantae Kim,*** and Hoi-Jun Yoo

IEEE ISCAS 2019

An Ultra-Low-Power Analog-Digital Hybrid CNN Face Recognition Processor Integrated with a CIS for Always-on Mobile Devices

► Ji-Hoon Kim, Changhyeon Kim, ***Kwantae Kim,*** and Hoi-Jun Yoo

IEEE ISSCC 2019
A 7.0fps Optical and Electrical Dual Tomographic Imaging SoC for Skin-Disease Diagnosis System
► Yongsu Lee, ***Kwantae Kim,*** Jiwon Lee, Kyung-Rog Lee, Surin Gweon, Minseo Kim, and Hoi-Jun Yoo
IEEE EMBC 2017
An Adaptive DC-Balanced and Multi-Mode Stimulator IC with 1GΩ Output Impedance for Compact Electro-Acupuncture System
► Jiwon Lee, Minseo Kim, ***Kwantae Kim,*** Kiseok Song, Sanghoon Lee, Weon Kim, Jong Shin Woo, and Hoi-Jun Yoo
IEEE ISSCC 2017
A 1.4-mΩ Sensitivity 94-dB Dynamic Range Electrical Impedance Tomography SoC and 48-Channel Hub SoC for 3D Lung Ventilation Monitoring System
► Minseo Kim, Hyunki Kim, Jaeeun Jang, Jihee Lee, Jaehyuk Lee, Jiwon Lee, Kyung-Rog Lee, ***Kwantae Kim,*** Yongsu Lee, and Hoi-Jun Yoo
IEEE ISSCC 2017
A 25.2mW EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring
► Unsoo Ha, Jaehyuk Lee, Jihee Lee, ***Kwantae Kim,*** Minseo Kim, Taehwan Roh, Sangsik Choi, and Hoi-Jun Yoo
IEEE ISSCC 2016
A 141μW Sensor SoC on OLED/OPD Substrate for SpO2/ExG Monitoring Sticker
► Yongsu Lee, Hyeonwoo Lee, Jaeeun Jang, Jihee Lee, Minseo Kim, Jaehyuk Lee, Hyunki Kim, Kyoung-Rog Lee, ***Kwantae Kim,*** Hyunwoo Cho, Seunghyup Yoo, and Hoi-Jun Yoo

Invited Talks

Samsung Research (Tech Talk) **CA, USA, Feb. 2019**
Abbott (Tech Talk) **CA, USA, Feb. 2019**

Skills

Programming Languages (MATLAB, TCL Script, Python)
Hardware Description Languages (HDL) (Verilog)
EDA Tools
Analog (Cadence Virtuoso, Calibre DRC, LVS, PEX)
Digital (Synopsys Design Compiler, IC Compiler)
Mixed-Signal (Cadence Virtuoso AMS)