ETH zürich

# The Era of Tiny IoT Platforms

## Integrated Circuits for Intelligent Biomedical/Neuromorphic Sensors


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Tuesday, April 23, 2024

# Outline

- Visions of IoT Sensors
- Biomedical Sensor
- Neuromorphic Sensor
- Outlook

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- **Visions of IoT Sensors**
- Biomedical Sensor
- Neuromorphic Sensor
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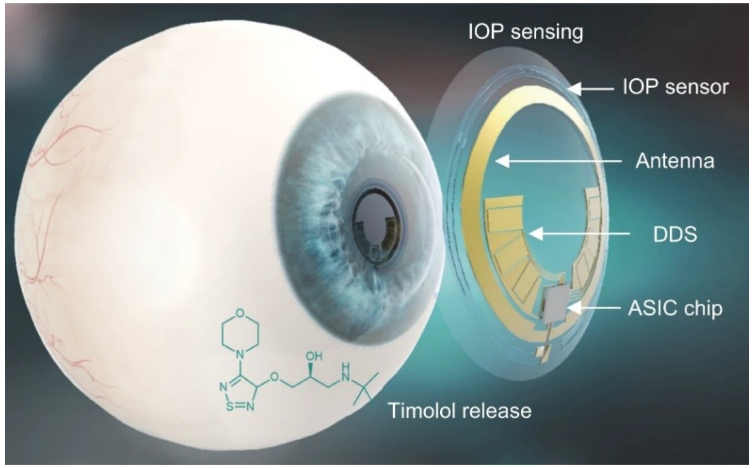
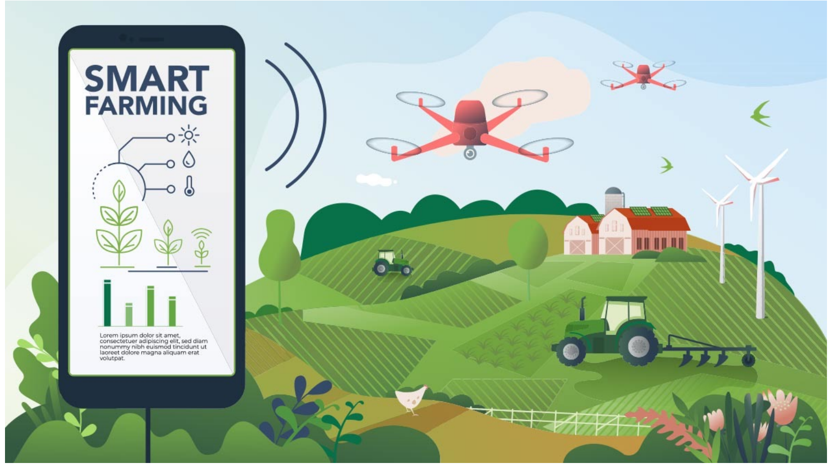
# Era of Internet of Things (IoT)

## Smart Healthcare



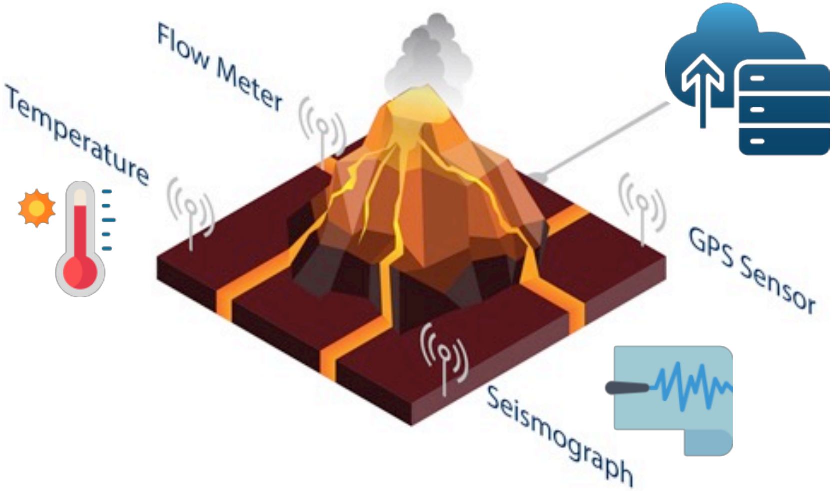

## Smart Farming



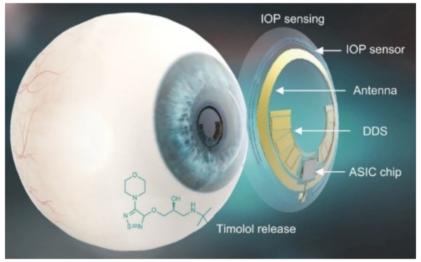

## Smart Pet Care

## Smart Factory

## Smart Environment



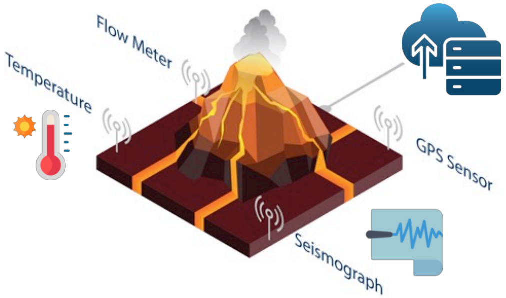
# Era of *Tiny* IoT Platforms


In the next 10 years,

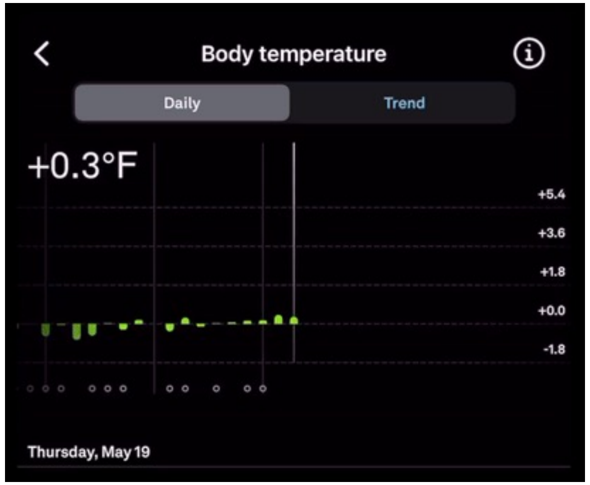
**1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless**

IoT platforms will enrich our daily lives!



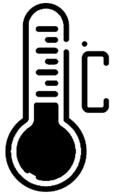
# **Example 1:** Bio-Signal Sensing

## 1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless



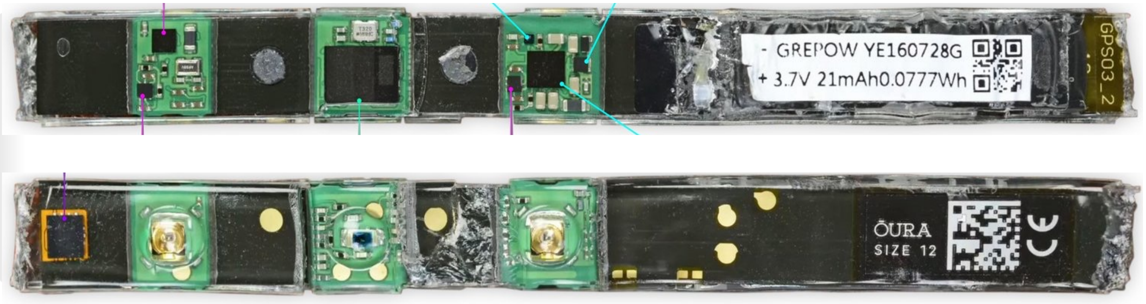

ŌURA

**Heart Rate**



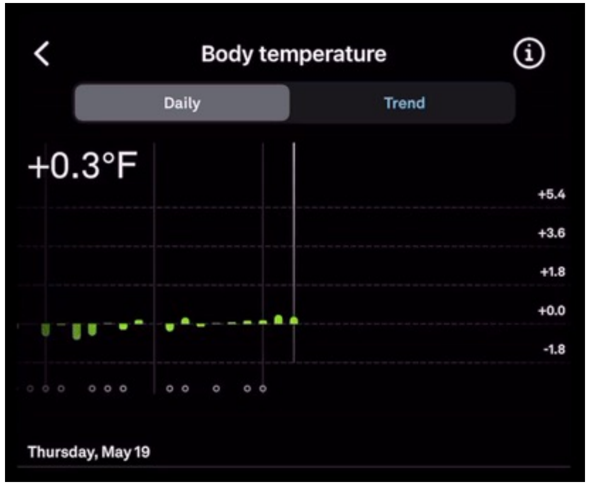
**Temp**

**PCB of Oura Ring 2**

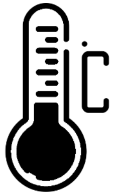


# **Example 1:** Bio-Signal Sensing

## 1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless




ŌURA



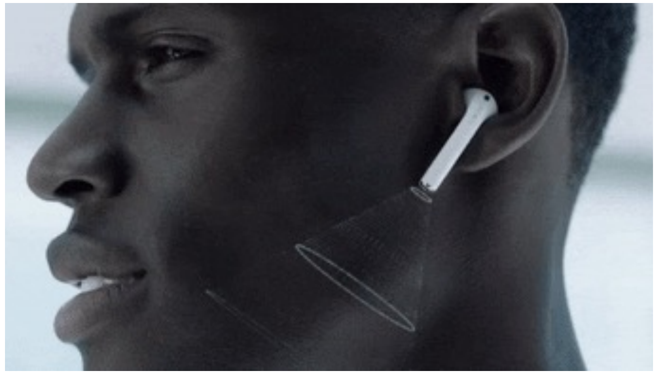
Heart Rate

Temp

SAMSUNG Galaxy Ring 2024

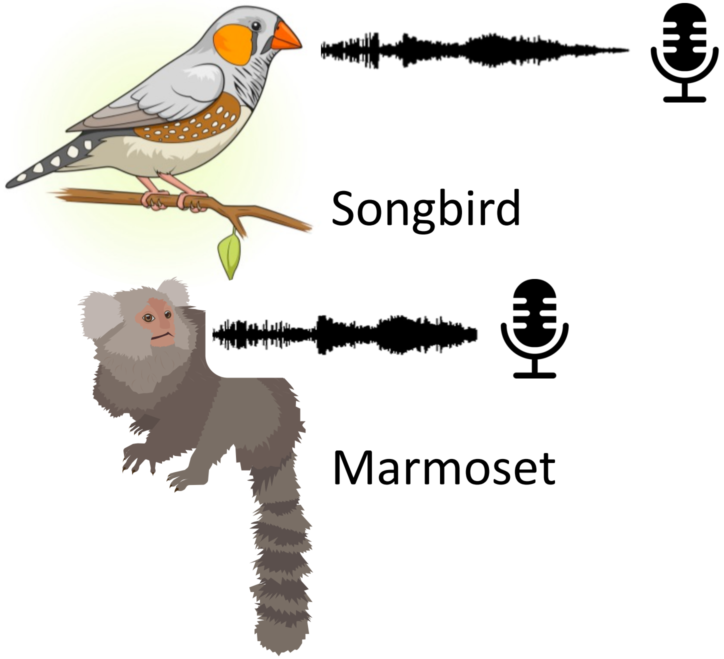
# **Example 2:** Audio Sensing

## 1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless



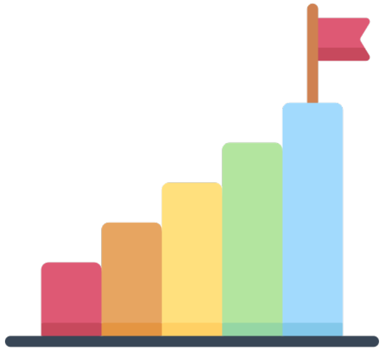
**Earbuds**

**Smart Home**




**Vocal Studies of Animals**

# Ultimate Research Goal

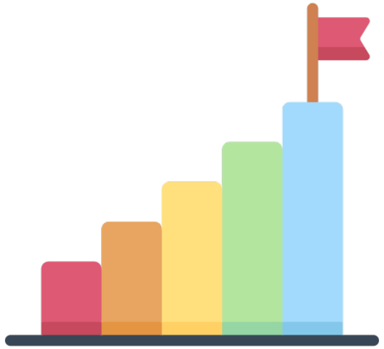


**Democratizing** the IoT platform with

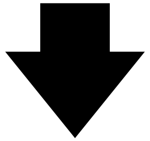
**1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless**

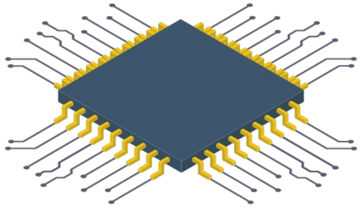
features to enrich our daily lives

# Ultimate Research Goal



**Democratizing** the IoT platform with
**1) Tiny + 2) Sensory + 3) Intelligent + 4) Wireless**
features to enrich our daily lives





We need **Highly Integrated System-on-Chip (SoC)**
under **Limited Energy Sources** and **Limited Silicon Area**

# Outline

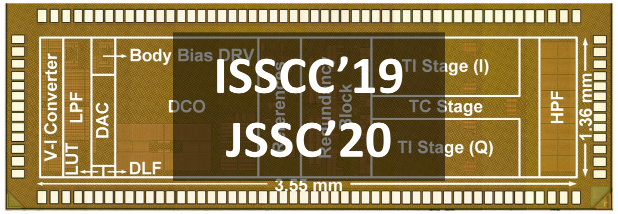
- Visions of IoT Sensors
- **Biomedical Sensor**
- **Neuromorphic Sensor**
- Outlook

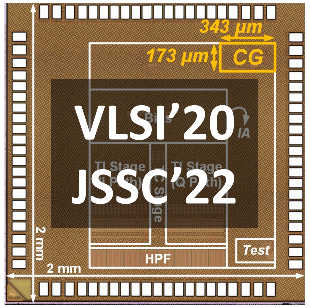
# Biomedical Sensor IC

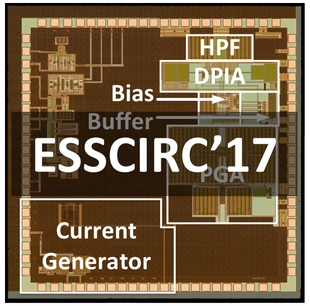
$$\text{BioZ} = \frac{V_{Sense}}{I_{Inject}}$$

**Ohm's Law**

$V = IR$ or $R = V/I$

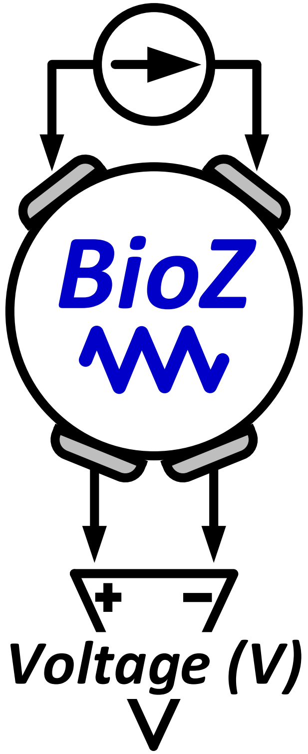
# Biomedical Sensor IC

$$\text{BioZ} = \frac{V_{\text{Sense}}}{I_{\text{Inject}}}$$

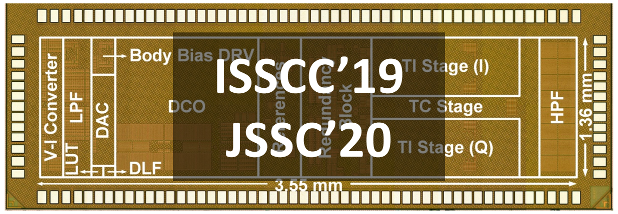
**Ohm's Law**

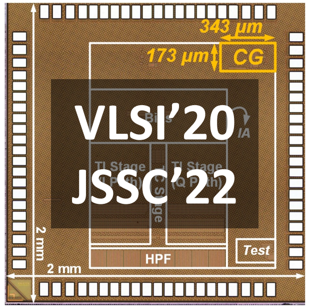
$V = IR$ or $R = V/I$

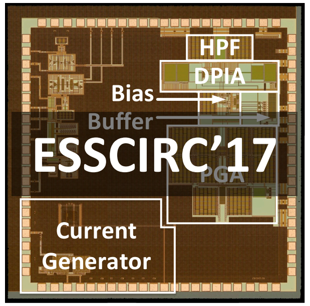
*Current (I)*




*Voltage (V)*

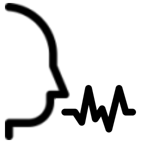


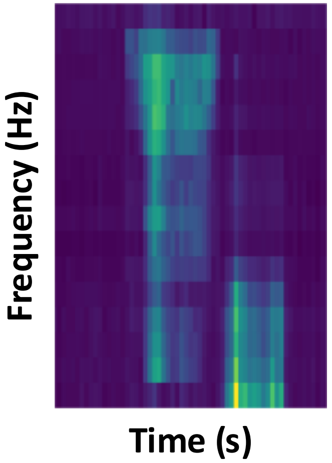




# Neuromorphic Sensor IC

**Mic.** **FEx** **DNN**

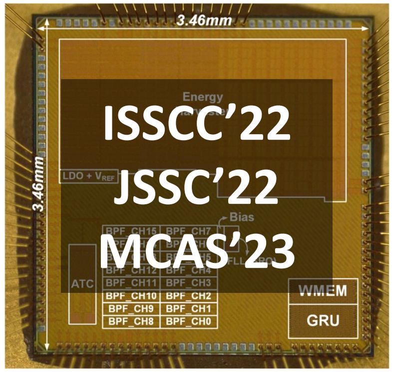


*"Yes"*




**Score**

| | |
|---|---|
| "Yes" | 0.95 |
| "Silence" | 0.02 |
| "Unknown" | 0.01 |
| "Down" | 0.01 |
| "Go" | 0.00 |
| ⋮ | |

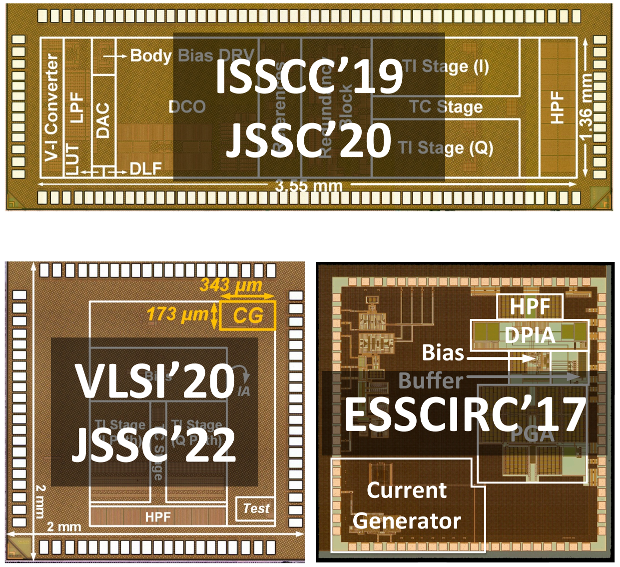


# Biomedical Sensor IC

$$\text{BioZ} = \frac{V_{Sense}}{I_{Inject}}$$

**Ohm's Law**

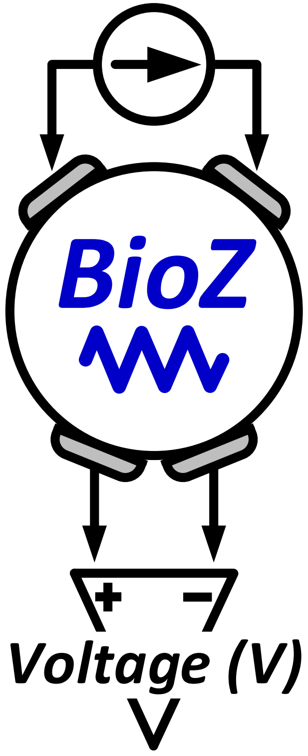
$V = IR$ or $R = V/I$


# Neuromorphic Sensor IC

# Bioimpedance (BioZ) Sensing

$$\text{BioZ} = \frac{V_{Sense}}{I_{Inject}}$$




Very Tiny Amplitude
<100mΩ$_{RMS}$ Resolution[1]

Even Finer Resolution
is Needed!

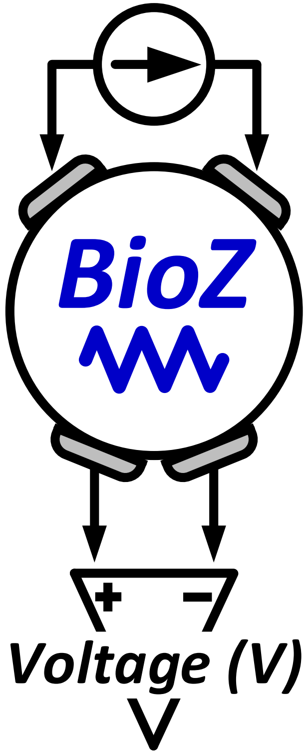

Miniaturization

[1]H. Ha, SSC-L 2018

# Bioimpedance (BioZ) Sensing

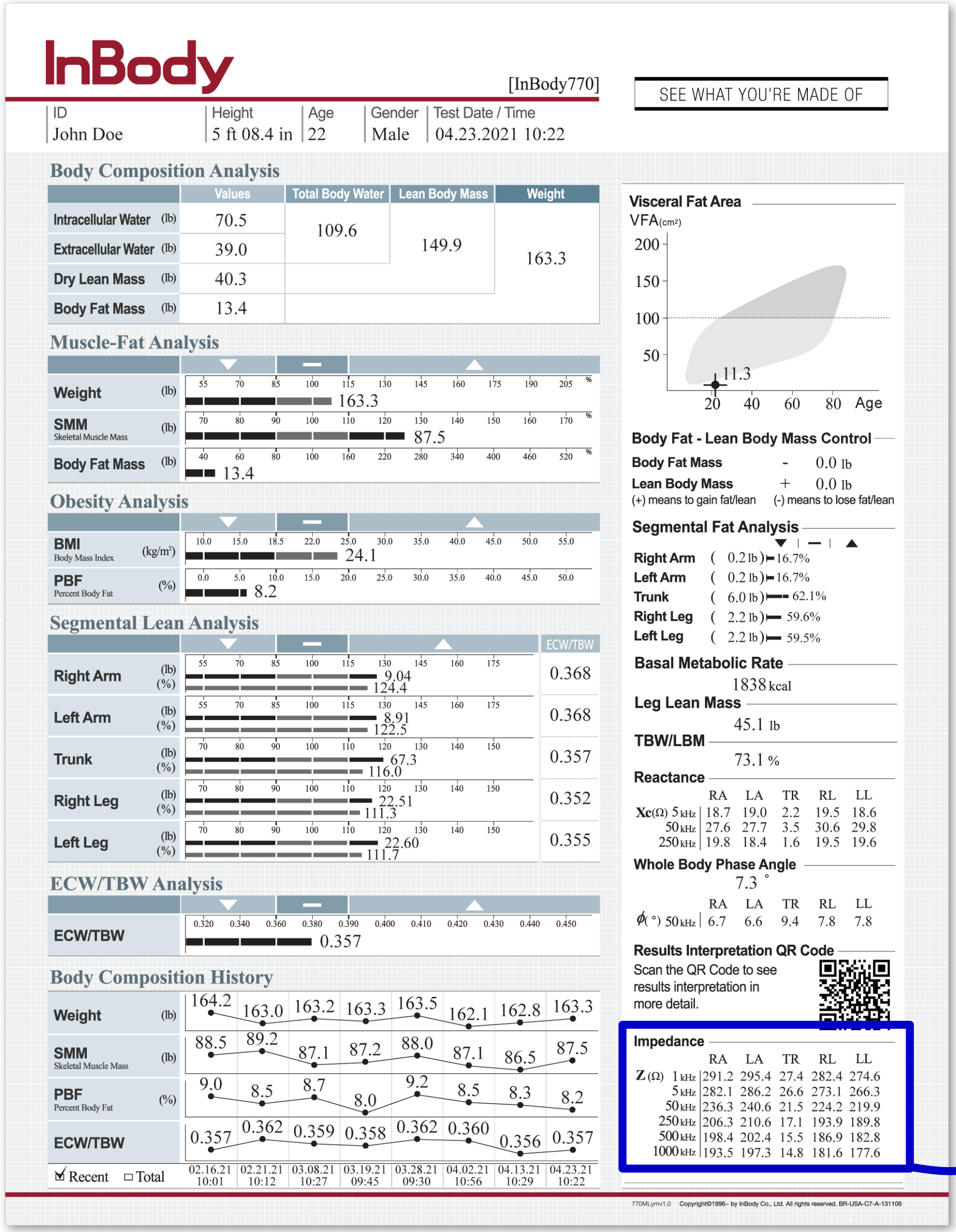
$$BioZ = \frac{V_{Sense}}{I_{Inject}}$$

*Current (I)*




*Voltage (V)*

H. P. Schwan, EMBC 1994


InBody [InBody770]

SEE WHAT YOU'RE MADE OF

| ID | Height | Age | Gender | Test Date / Time |
|---|---|---|---|---|
| John Doe | 5 ft 08.4 in | 22 | Male | 04.23.2021 10:22 |

**Body Composition Analysis**

| | Values | Total Body Water | Lean Body Mass | Weight |
|---|---|---|---|---|
| Intracellular Water (lb) | 70.5 | 109.6 | 149.9 | 163.3 |
| Extracellular Water (lb) | 39.0 | | | |
| Dry Lean Mass (lb) | 40.3 | | | |
| Body Fat Mass (lb) | 13.4 | | | |

**Muscle-Fat Analysis**

Weight (lb) 163.3
SMM Skeletal Muscle Mass (lb) 87.5
Body Fat Mass (lb) 13.4

**Obesity Analysis**

BMI Body Mass Index (kg/m²) 24.1
PBF Percent Body Fat (%) 8.2

**Segmental Lean Analysis**

| | (lb) | (%) | ECW/TBW |
|---|---|---|---|
| Right Arm | 9.04 | 124.4 | 0.368 |
| Left Arm | 8.91 | 122.5 | 0.368 |
| Trunk | 67.3 | 116.0 | 0.357 |
| Right Leg | 22.51 | 111.3 | 0.352 |
| Left Leg | 22.60 | 111.7 | 0.355 |

**ECW/TBW Analysis**

ECW/TBW 0.357

**Body Composition History**

| | 02.16.21 10:01 | 02.21.21 10:12 | 03.08.21 10:27 | 03.19.21 09:45 | 03.28.21 09:30 | 04.02.21 10:56 | 04.13.21 10:29 | 04.23.21 10:22 |
|---|---|---|---|---|---|---|---|---|
| Weight (lb) | 164.2 | 163.0 | 163.2 | 163.3 | 163.5 | 162.1 | 162.8 | 163.3 |
| SMM Skeletal Muscle Mass (lb) | 88.5 | 89.2 | 87.1 | 87.2 | 88.0 | 87.1 | 86.5 | 87.5 |
| PBF Percent Body Fat (%) | 9.0 | 8.5 | 8.7 | 8.0 | 9.2 | 8.5 | 8.3 | 8.2 |
| ECW/TBW | 0.357 | 0.362 | 0.359 | 0.358 | 0.362 | 0.360 | 0.356 | 0.357 |

☑ Recent ☐ Total

**Visceral Fat Area**

VFA (cm²) 11.3

**Body Fat - Lean Body Mass Control**

Body Fat Mass − 0.0 lb
Lean Body Mass + 0.0 lb
(+) means to gain fat/lean (-) means to lose fat/lean

**Segmental Fat Analysis**

Right Arm (0.2 lb) 16.7%
Left Arm (0.2 lb) 16.7%
Trunk (6.0 lb) 62.1%
Right Leg (2.2 lb) 59.6%
Left Leg (2.2 lb) 59.5%

**Basal Metabolic Rate**

1838 kcal

**Leg Lean Mass**

45.1 lb

**TBW/LBM**

73.1 %

**Reactance**

| Xc(Ω) | RA | LA | TR | RL | LL |
|---|---|---|---|---|---|
| 5 kHz | 18.7 | 19.0 | 2.2 | 19.5 | 18.6 |
| 50 kHz | 27.6 | 27.7 | 3.5 | 30.6 | 29.8 |
| 250 kHz | 19.8 | 18.4 | 1.6 | 19.5 | 19.6 |

**Whole Body Phase Angle**

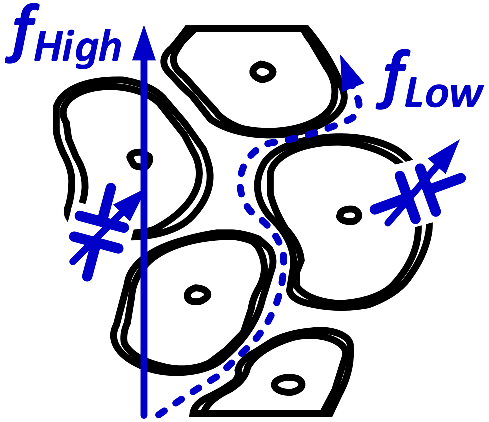
7.3 °

| ϕ(°) | RA | LA | TR | RL | LL |
|---|---|---|---|---|---|
| 50 kHz | 6.7 | 6.6 | 9.4 | 7.8 | 7.8 |

**Results Interpretation QR Code**

Scan the QR Code to see results interpretation in more detail.



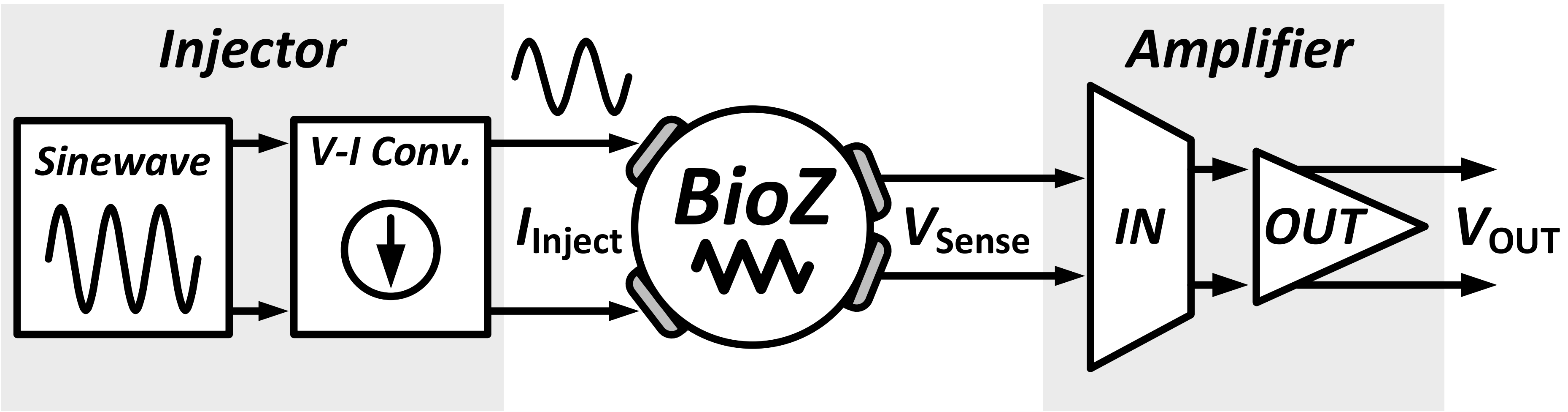



## Impedance

| Z (Ω) | RA | LA | TR | RL | LL |
|---|---|---|---|---|---|
| 1 kHz | 291.2 | 295.4 | 27.4 | 282.4 | 274.6 |
| 5 kHz | 282.1 | 286.2 | 26.6 | 273.1 | 266.3 |
| 50 kHz | 236.3 | 240.6 | 21.5 | 224.2 | 219.9 |
| 250 kHz | 206.3 | 210.6 | 17.1 | 193.9 | 189.8 |
| 500 kHz | 198.4 | 202.4 | 15.5 | 186.9 | 182.8 |
| 1000 kHz | 193.5 | 197.3 | 14.8 | 181.6 | 177.6 |

# Bioimpedance (BioZ) Sensing

$$\text{BioZ} = \frac{V_{Sense}}{I_{Inject}}$$


**Current Injector Needs:**

**Pure Sinewave**
(Total Harmonic Distortion (THD) < 1%)
**Low Power** (<10µW)
**Low Area** (Smaller is Better)

**Voltage Amplifier Needs:**

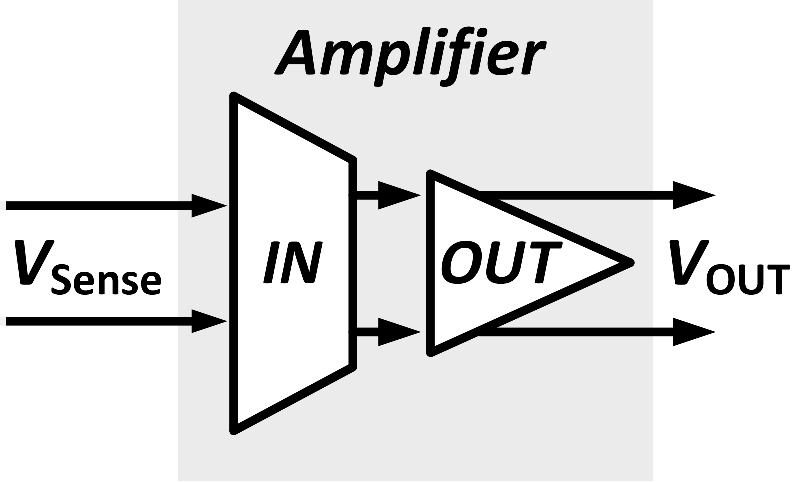
**Low Noise** (<100nV/√Hz)
**Wide Bandwidth** (>100kHz)
**Low Power** (<10µW)

# Bioimpedance (BioZ) Sensing

$$\text{BioZ} = \frac{V_{Sense}}{I_{Inject}}$$





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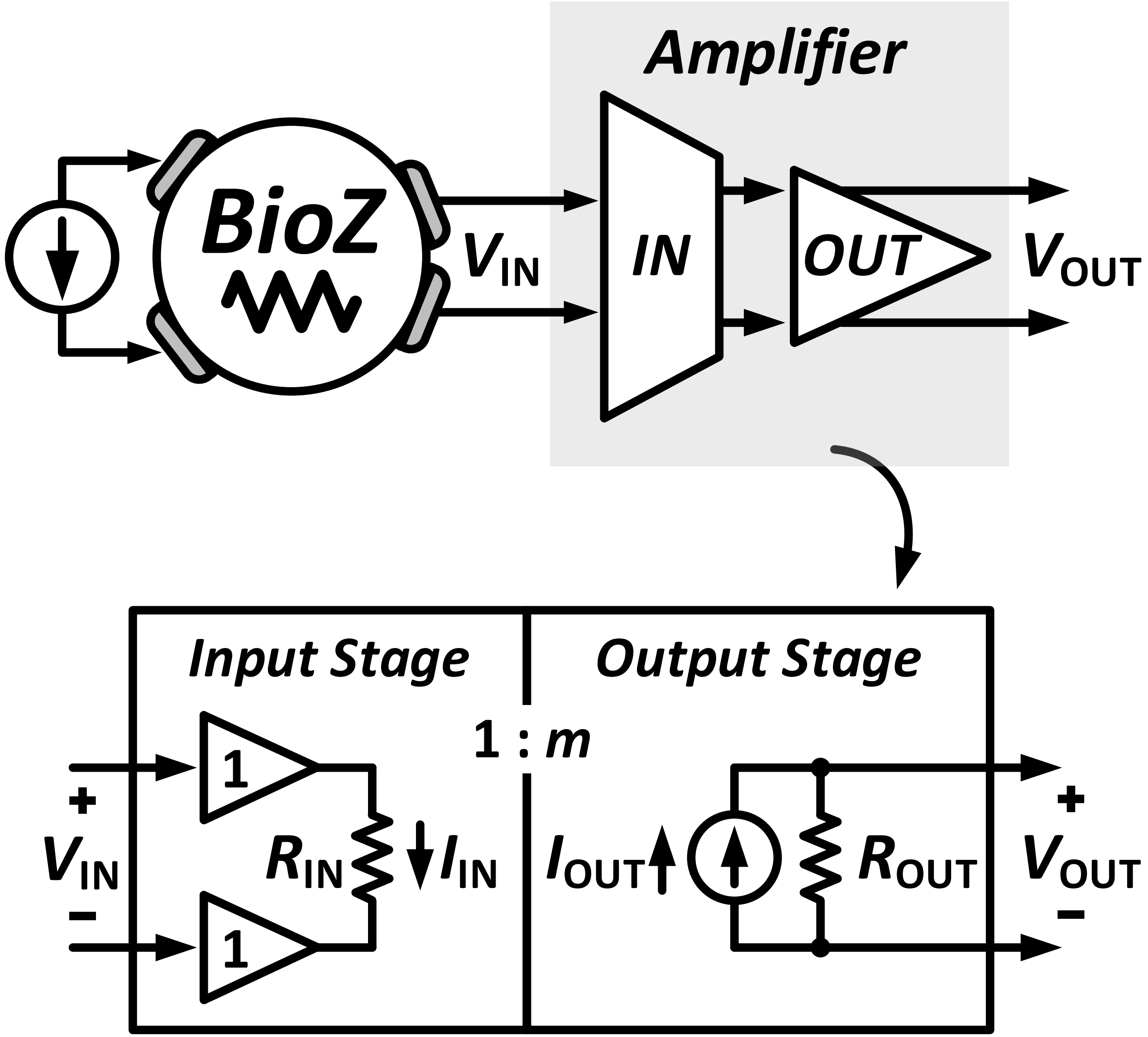
# Voltage Readout Amplifier

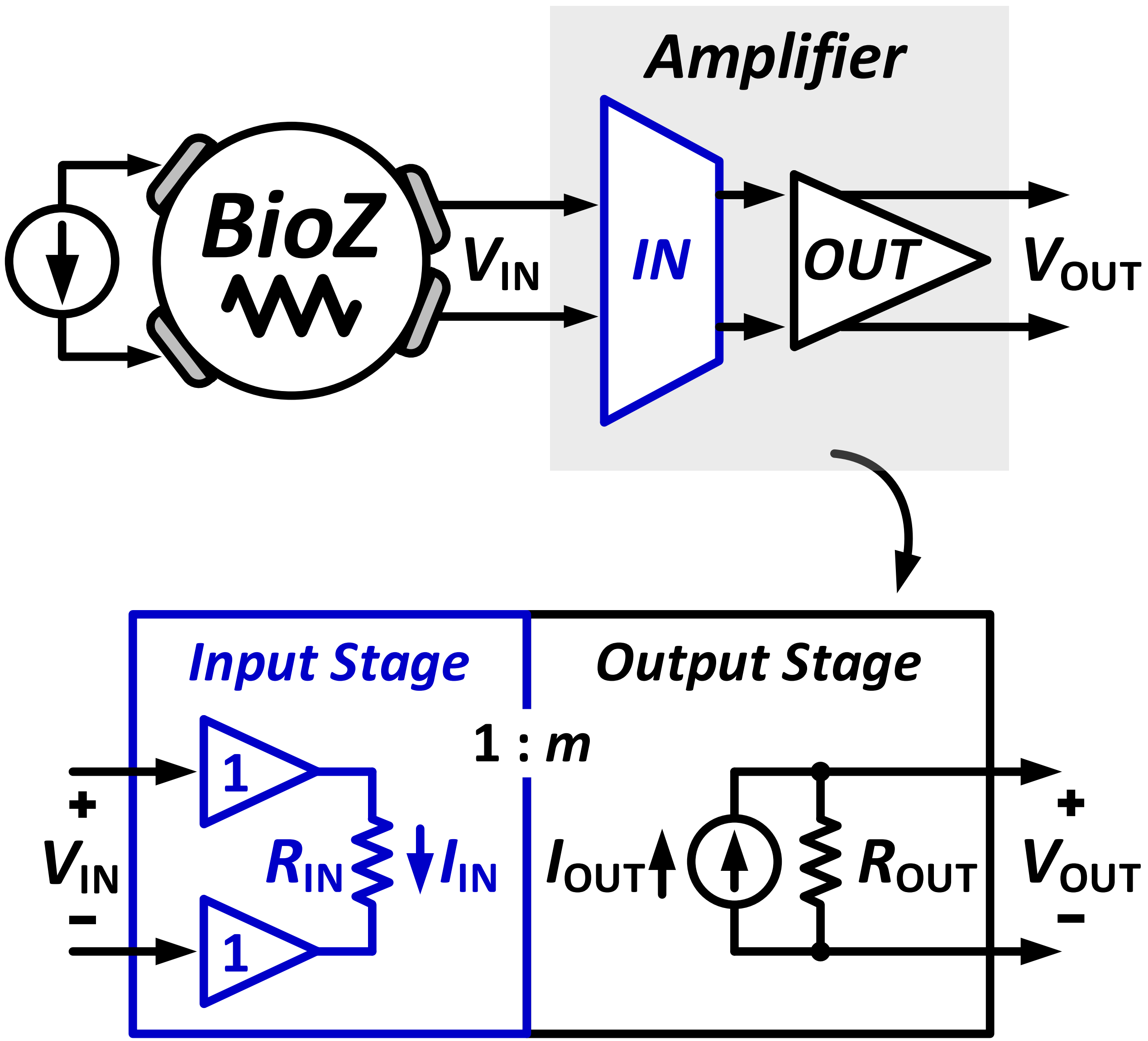



**Amplifier Gain**

$$A_v = m\,\frac{R_{OUT}}{R_{IN}}$$

N. V. Helleputte, ISSCC 2012

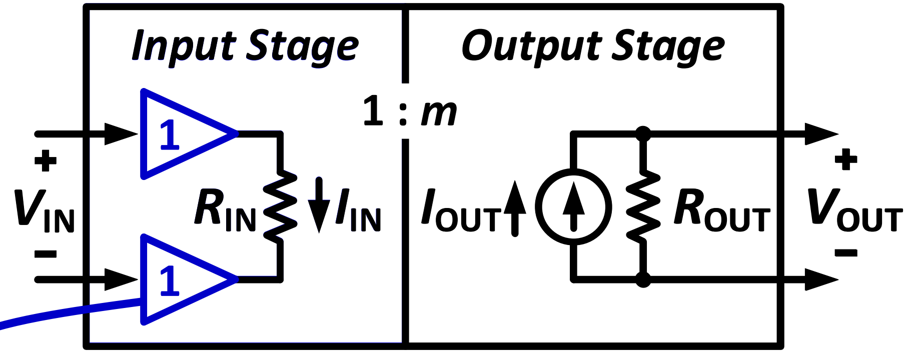
# Voltage Readout Amplifier

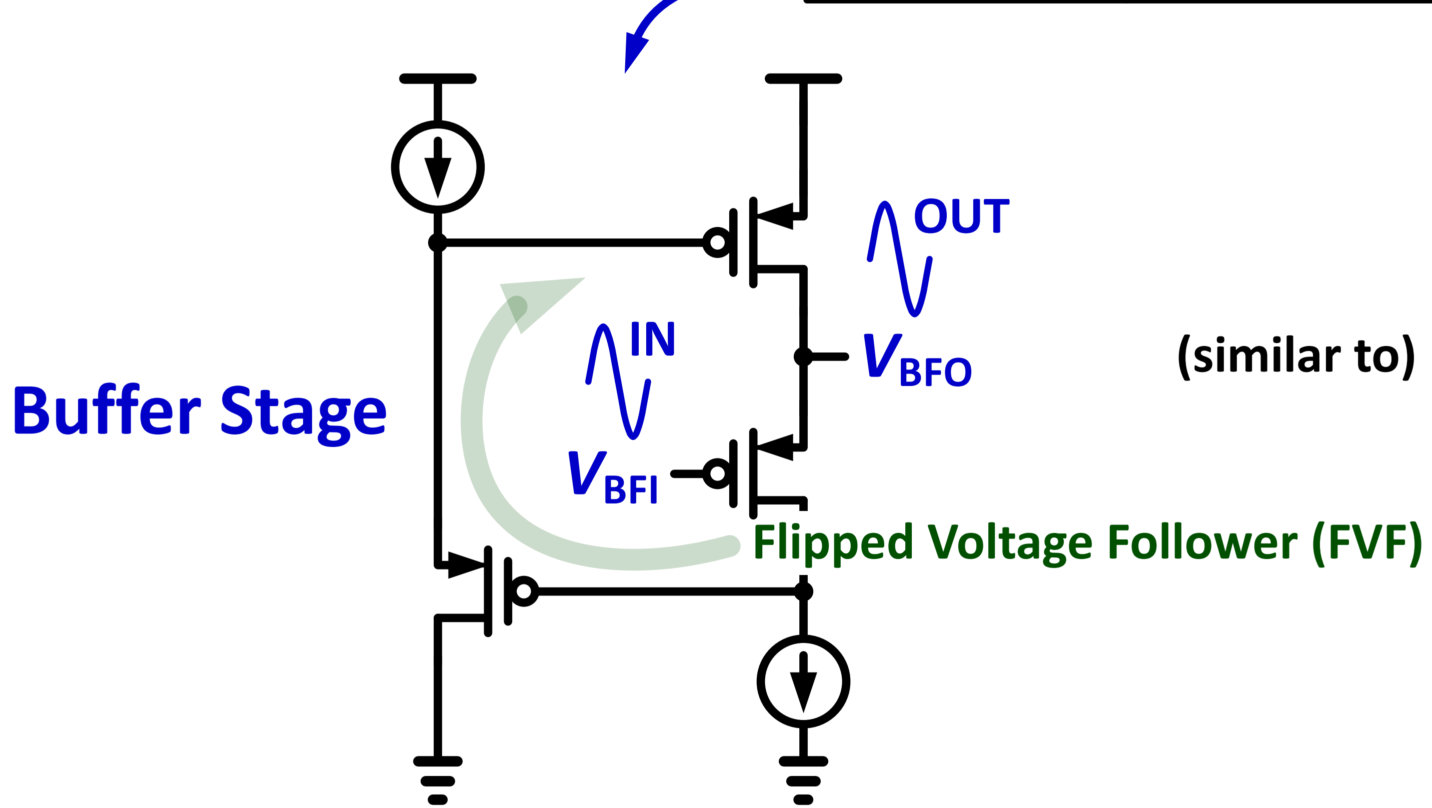



**Input Stage Determines Noise & BW Performance!**

N. V. Helleputte, ISSCC 2012

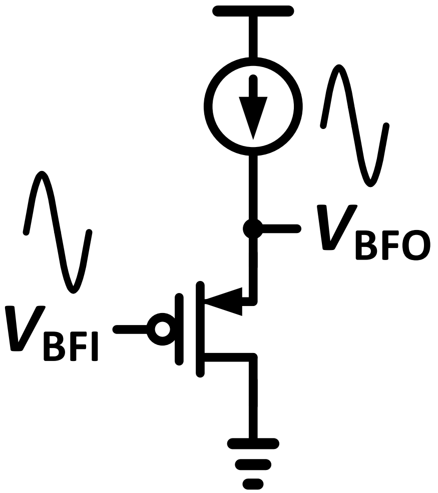
# Voltage Buffer



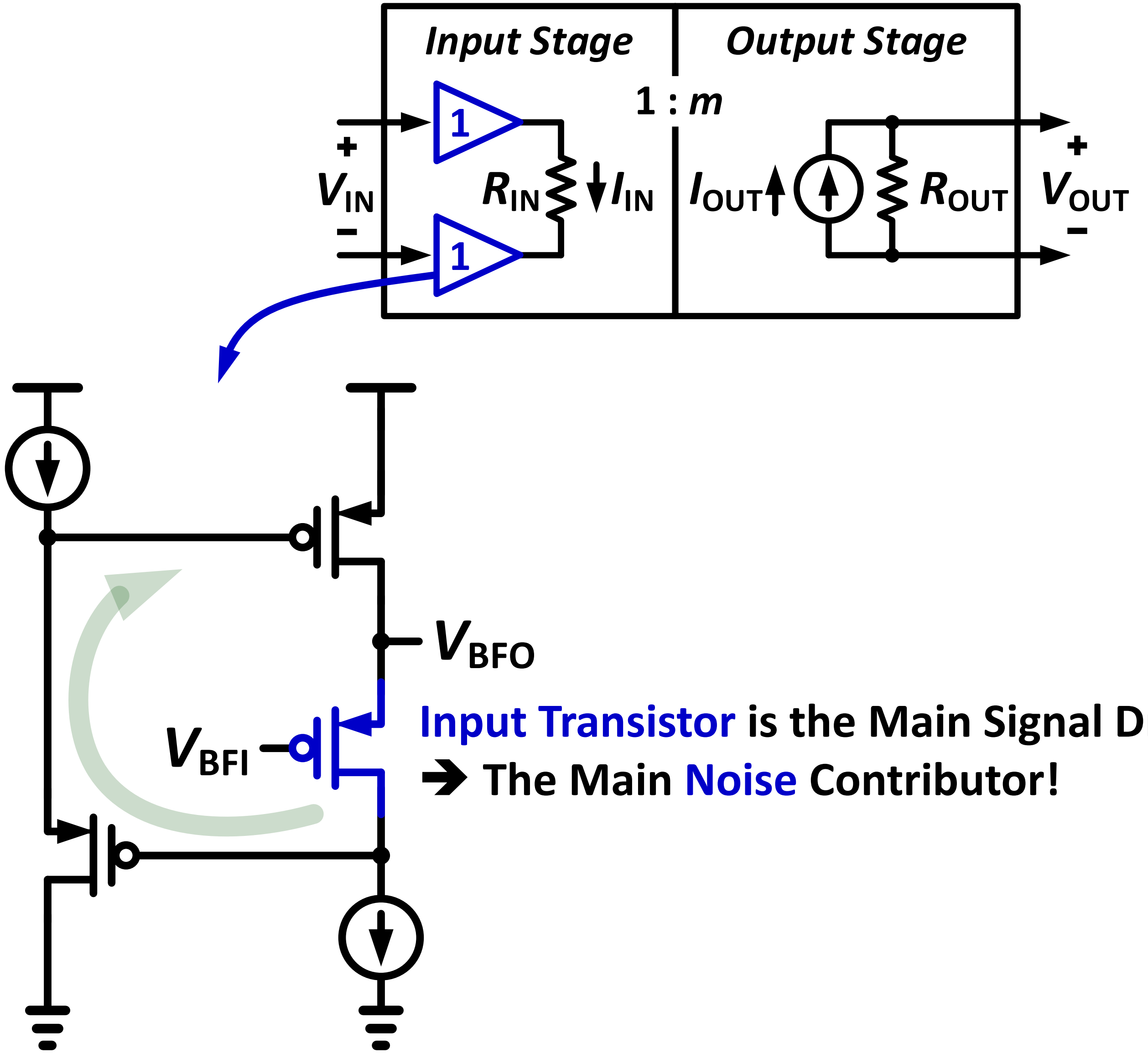

(similar to)

Source Follower



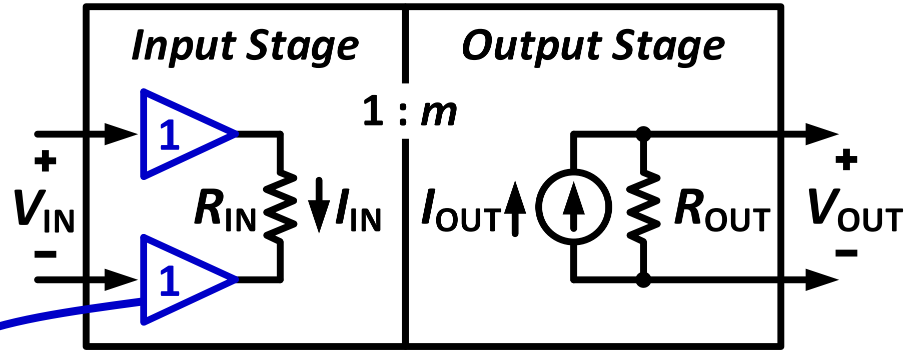

N. V. Helleputte, ISSCC 2012

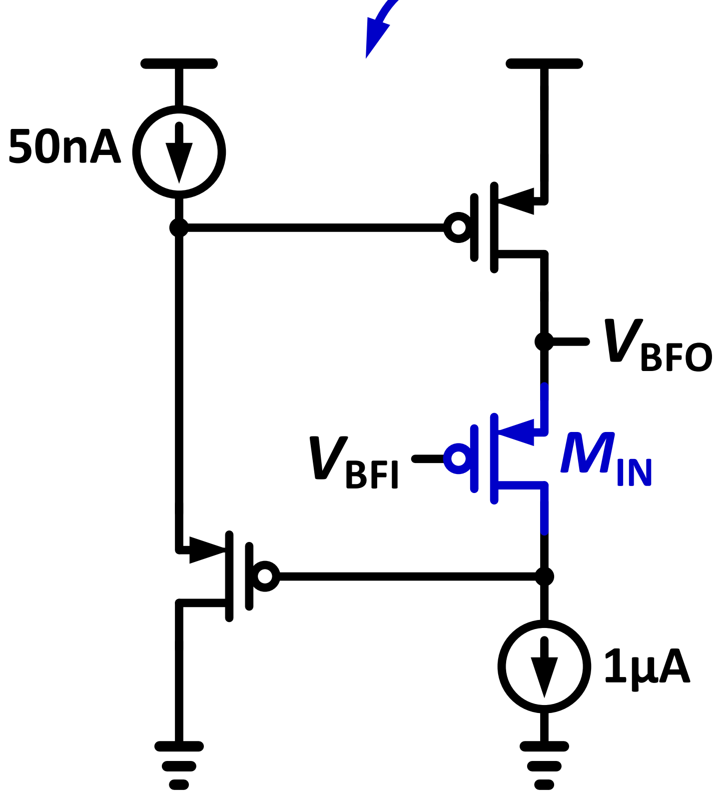
# Voltage Buffer: *Low-Noise* Design




Input Transistor is the Main Signal Driver
➔ The Main Noise Contributor!

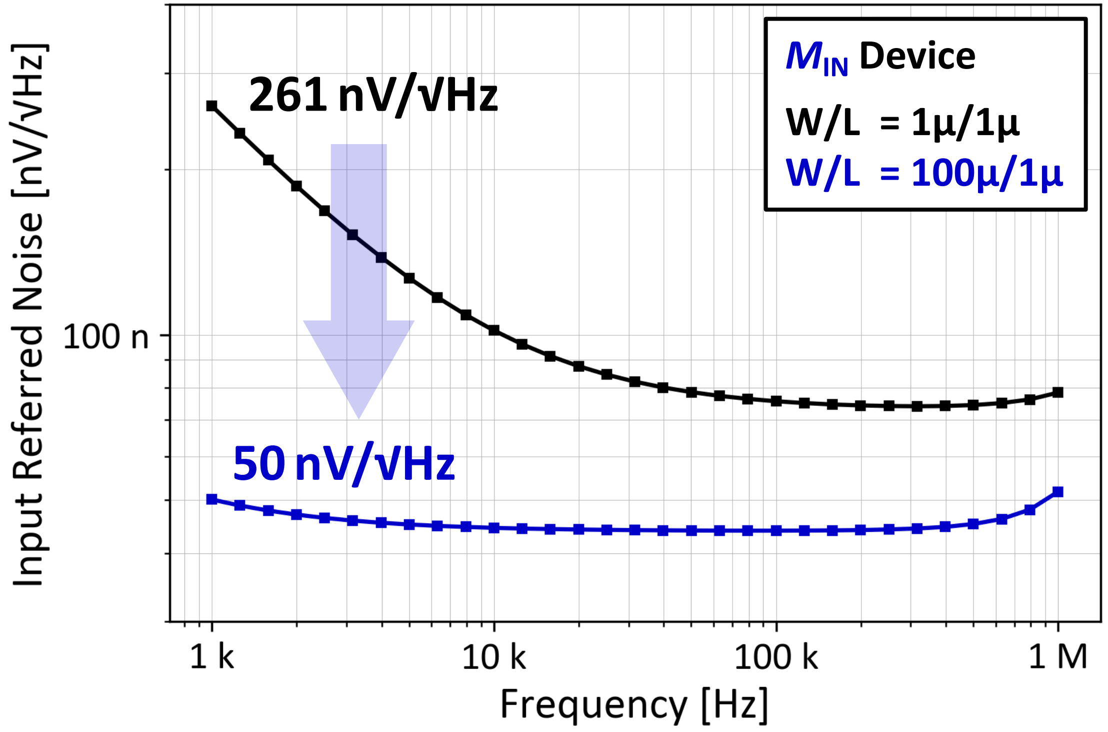
# Voltage Buffer: *Low-Noise* Design



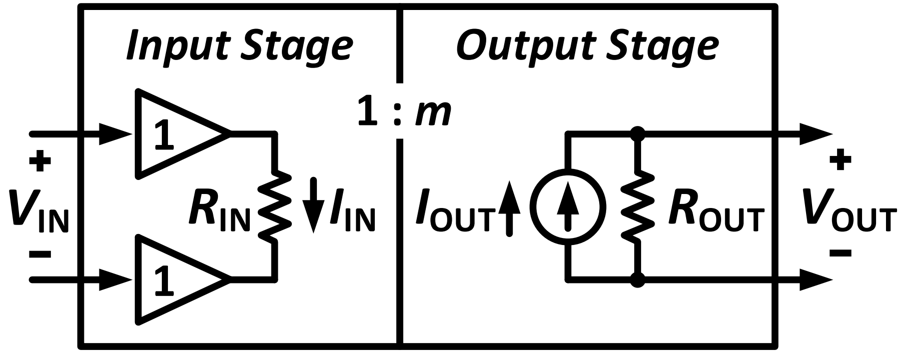



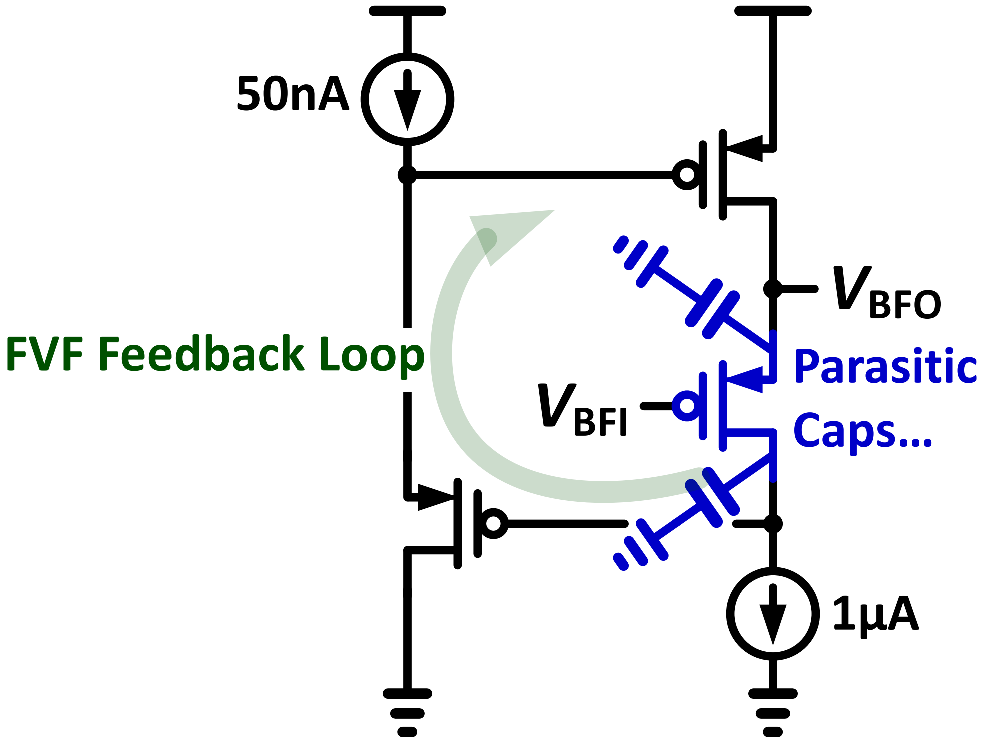

Thermal Flicker

$$V_n^2(f) = \frac{8}{3}\frac{kT}{g_m} + \frac{K}{C_{ox}WL}\frac{1}{f} \quad [\mathrm{V^2/Hz}]$$

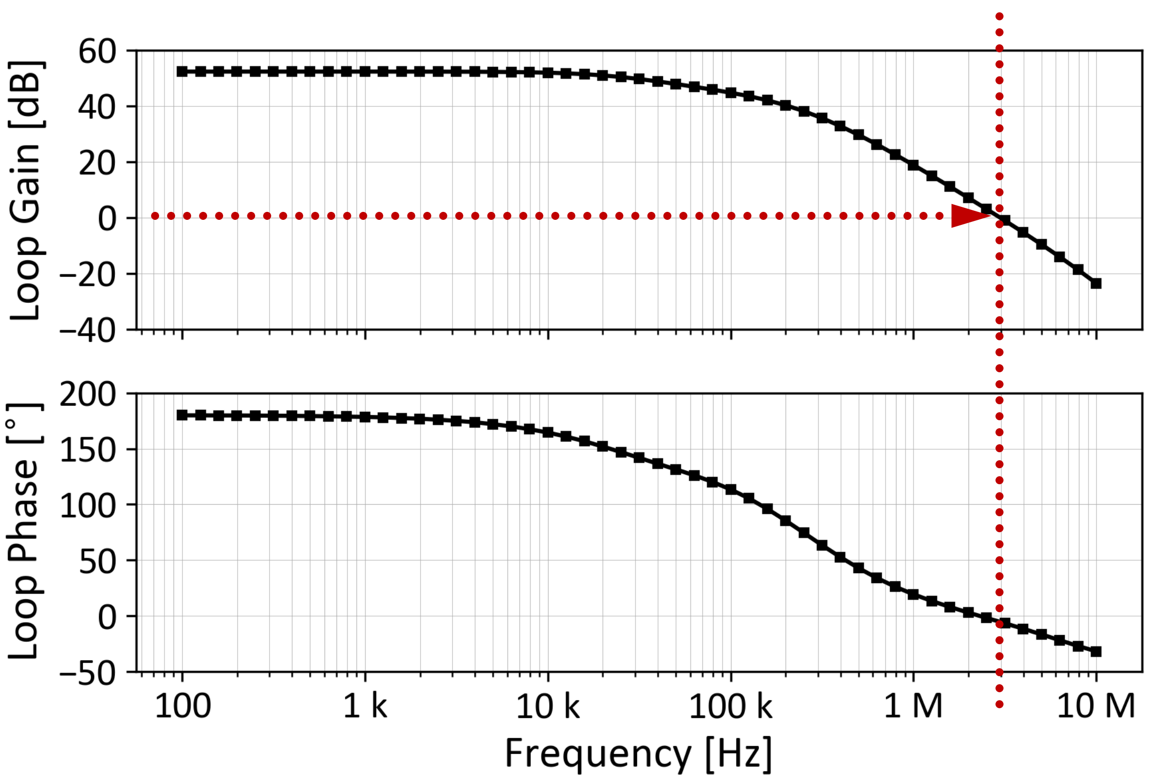


# Voltage Buffer: *Feedback Stability*




Phase Margin = -5.28°
➔ Unstable!



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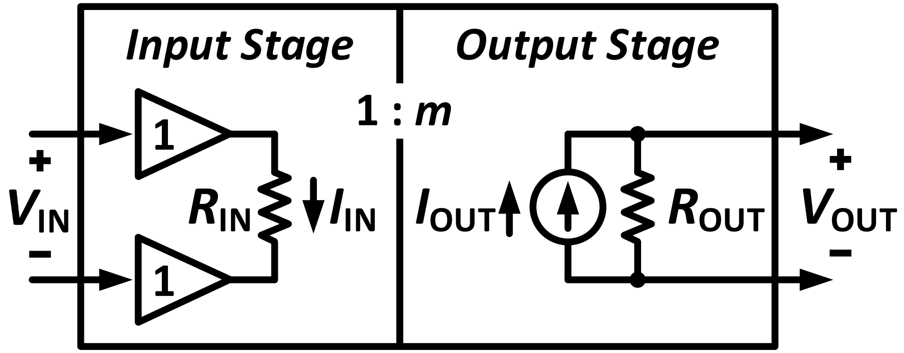
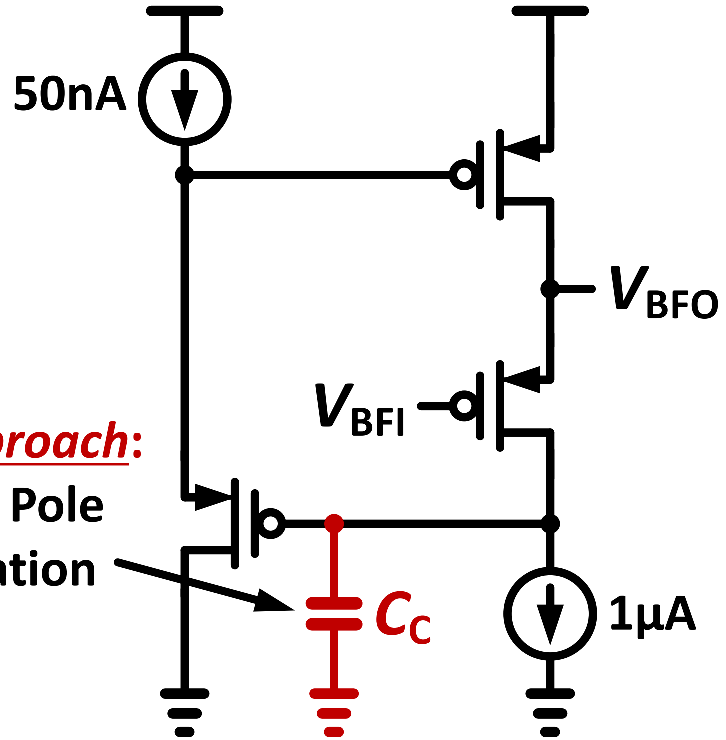
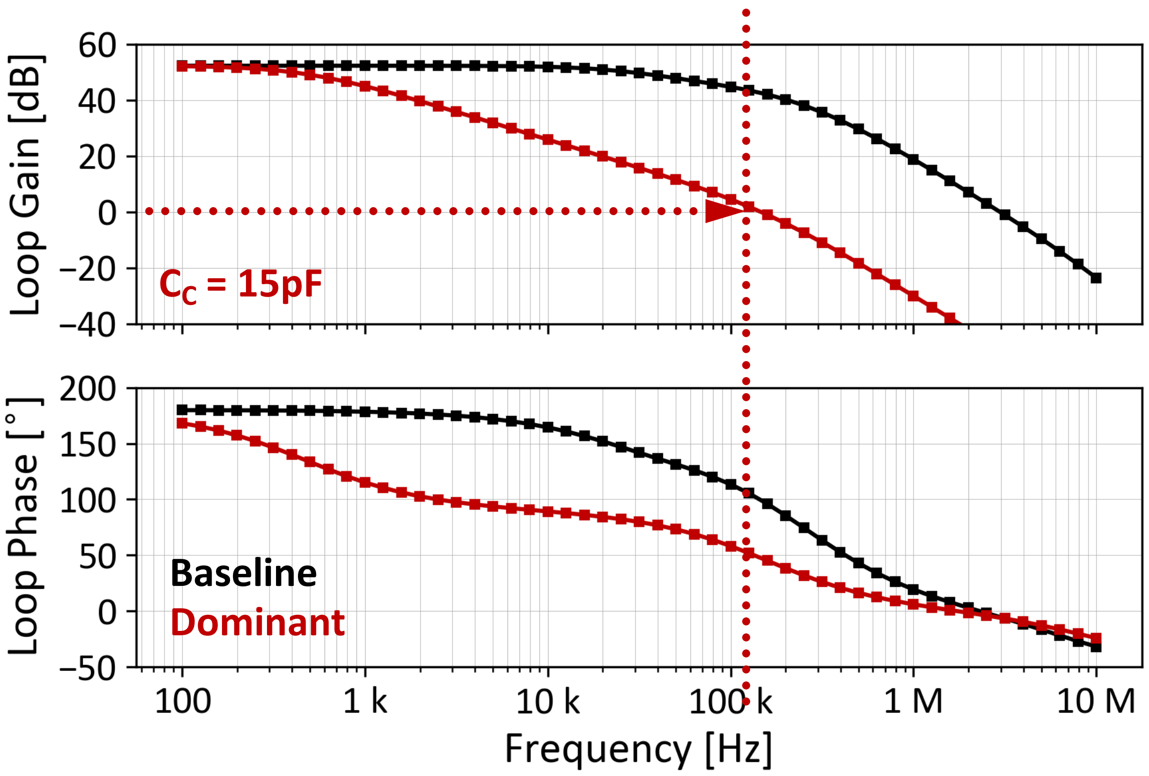


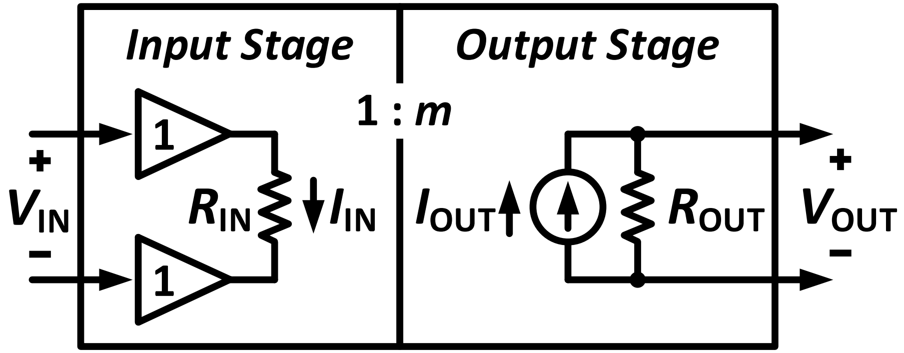



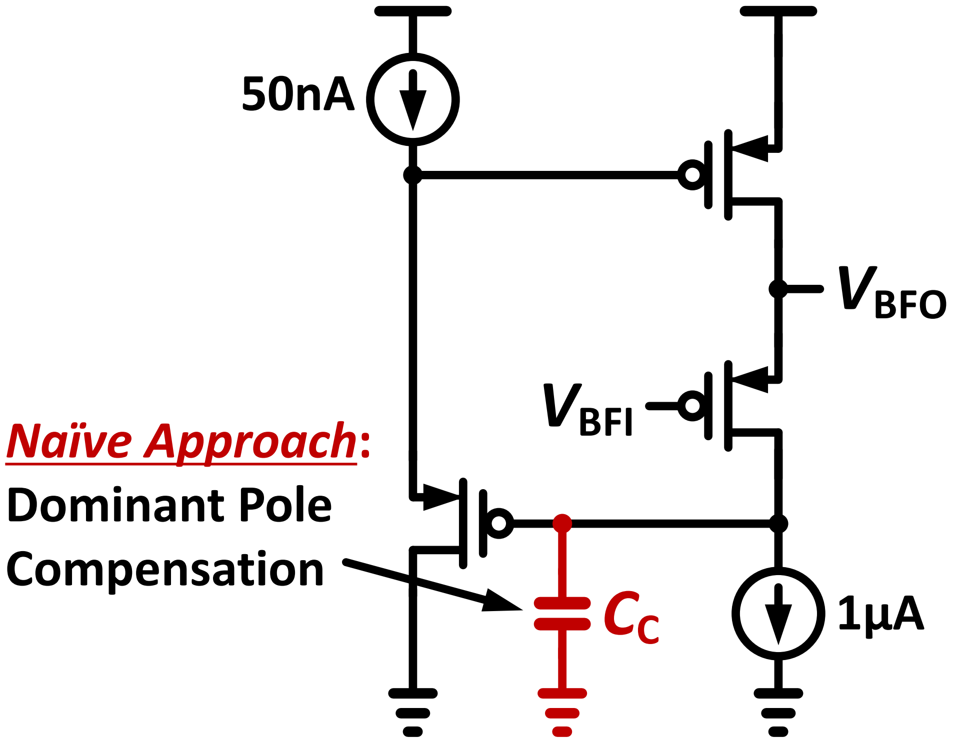

***Naïve Approach***:
Dominant Pole Compensation

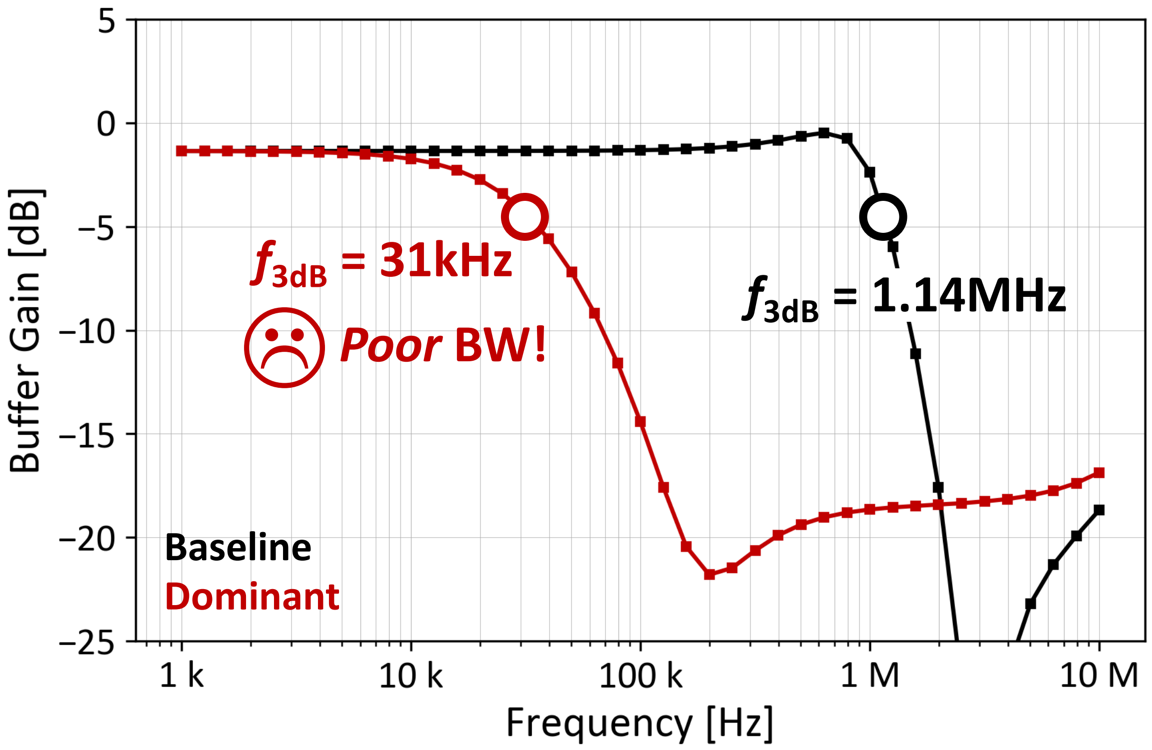
**Phase Margin = 47°**
➔ This is okay, but …



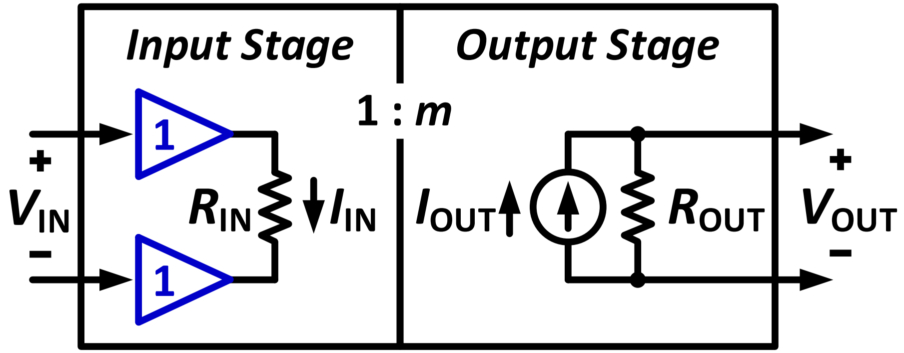
# Voltage Buffer: *Bandwidth Problem*



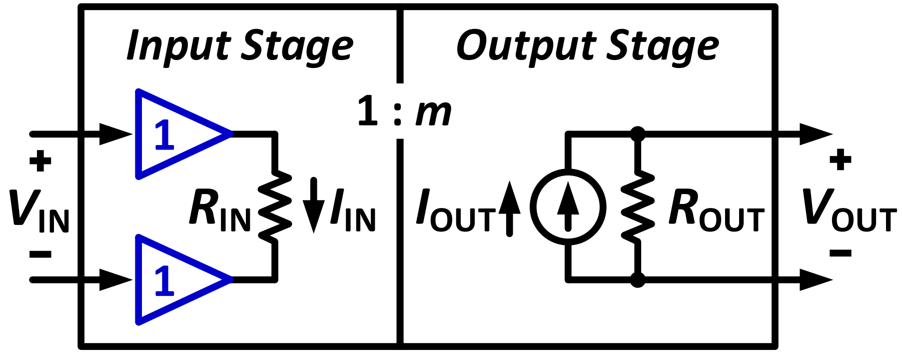
# Voltage Buffer

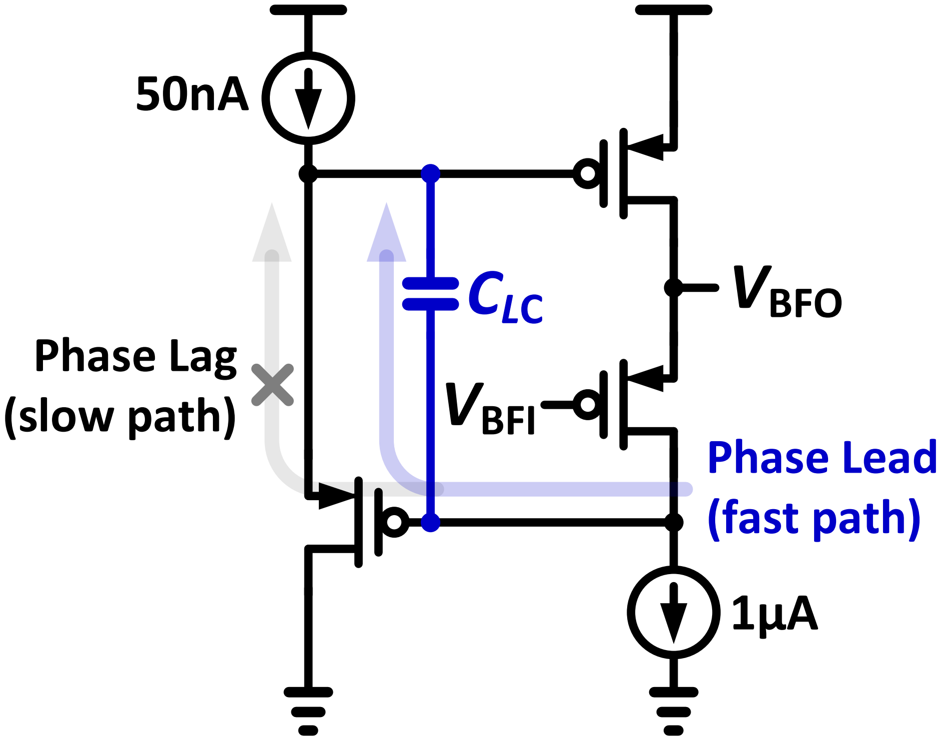



## Design Dilemma:

- ✔ **Low Noise** (<100nV/√Hz)
- ✔ **Low Power** (<10µW)
- ✔ **Stability** (PM > 50º)
- ✘ **Bandwidth** (>100kHz)

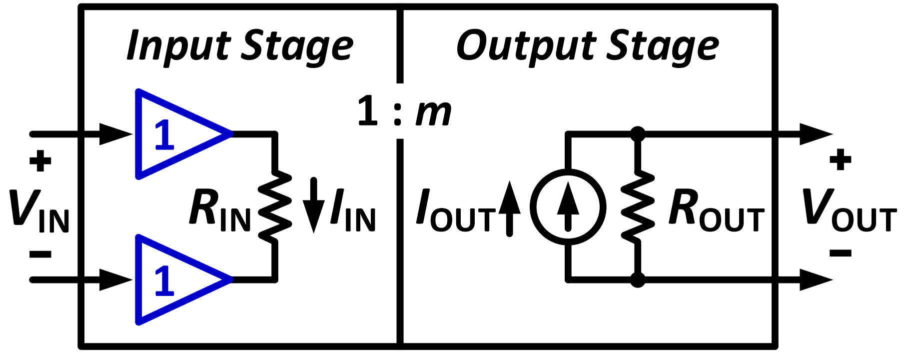
# Voltage Buffer: *Lead Compensation (LC)*[1]

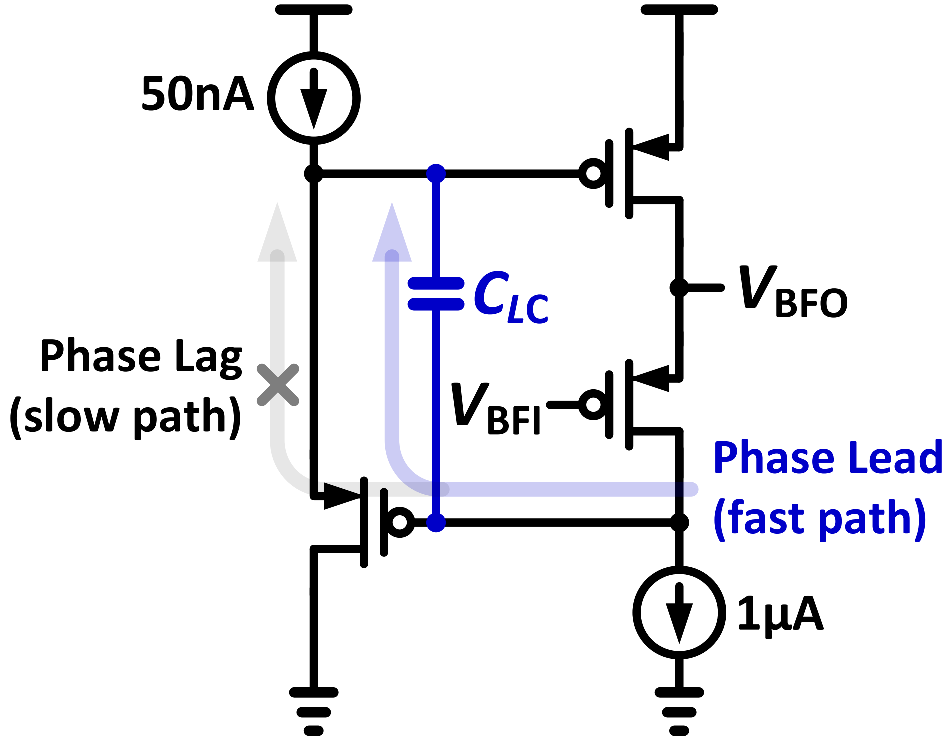


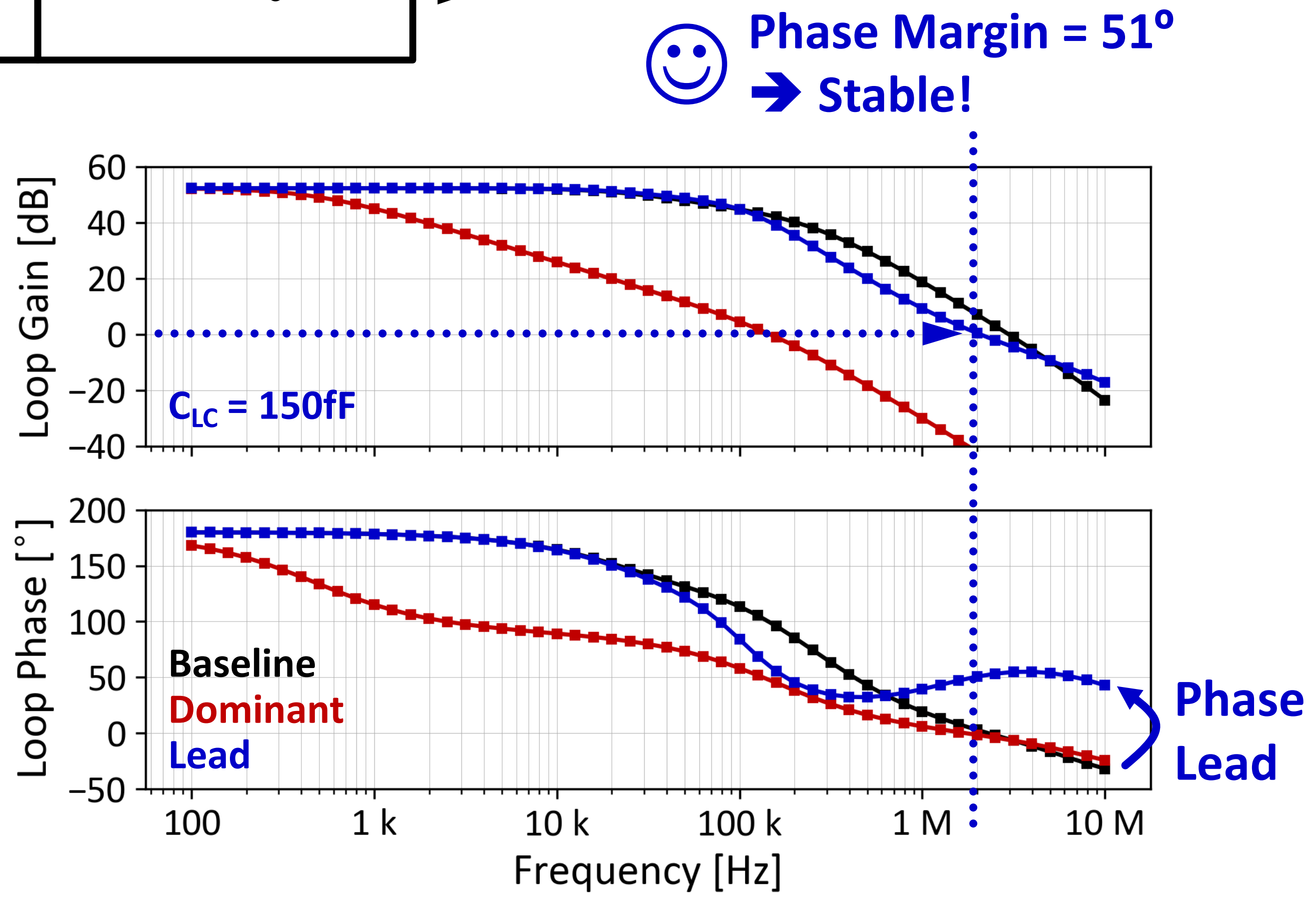




[1]K. Kim, ISSCC 2019 + JSSC 2020

# Voltage Buffer: *Lead Compensation (LC)*[1]

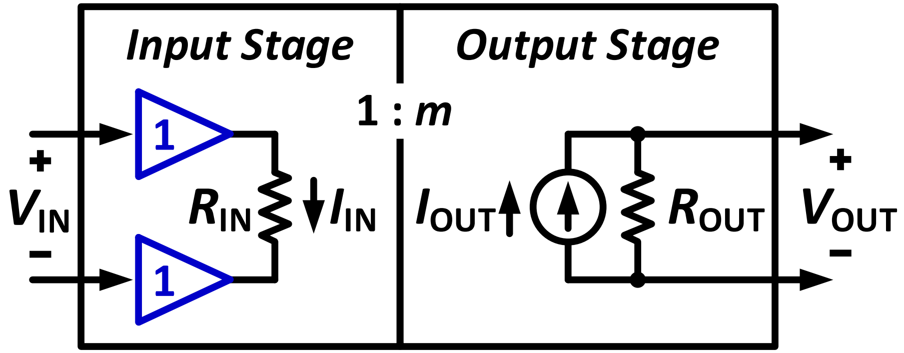


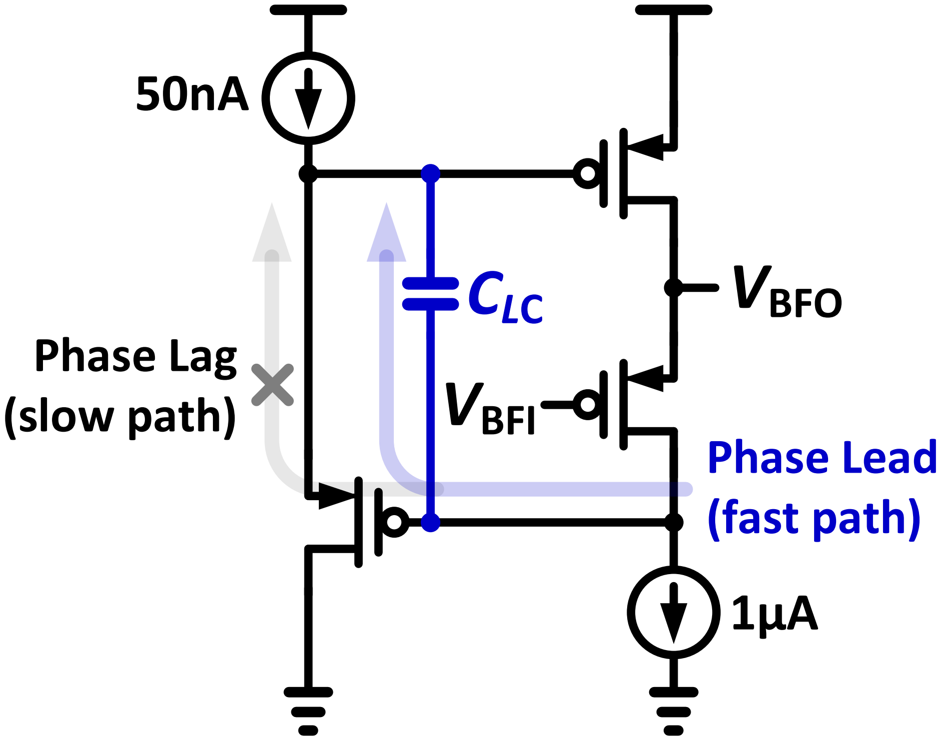



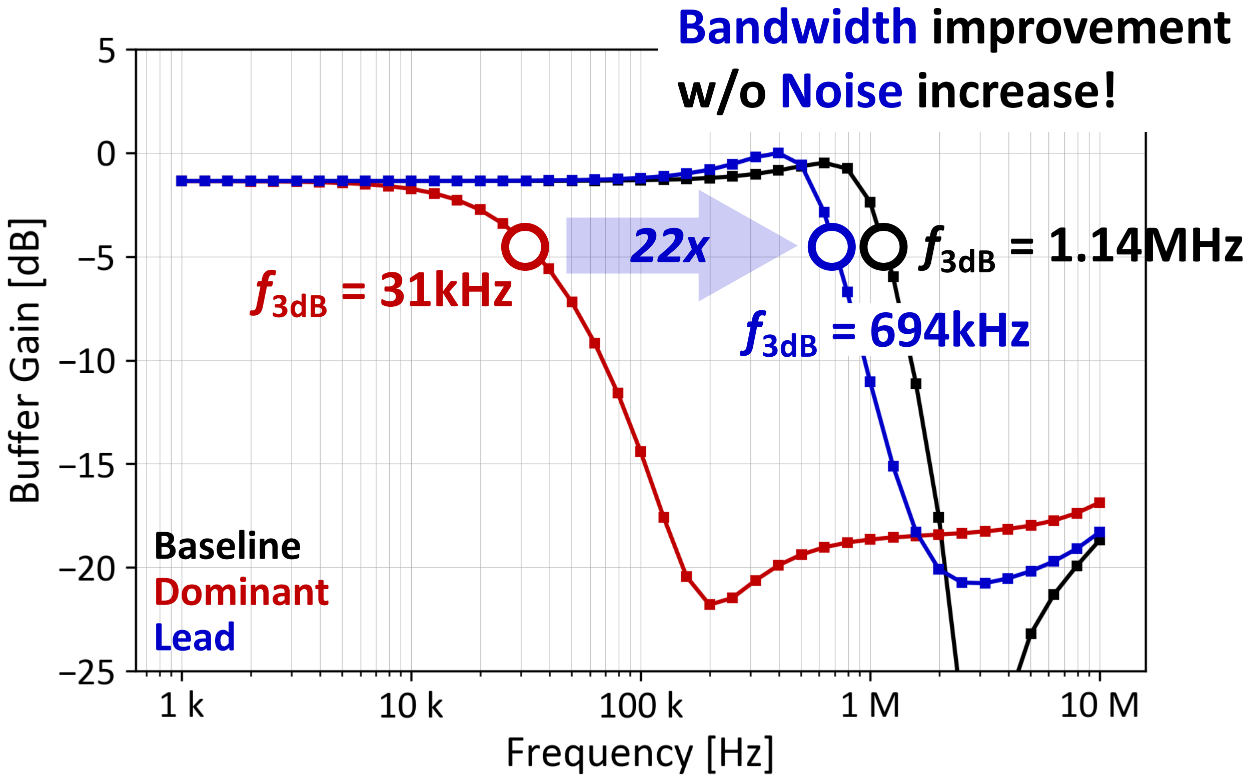




[1]K. Kim, ISSCC 2019 + JSSC 2020

# Voltage Buffer: *Lead Compensation (LC)*[1]

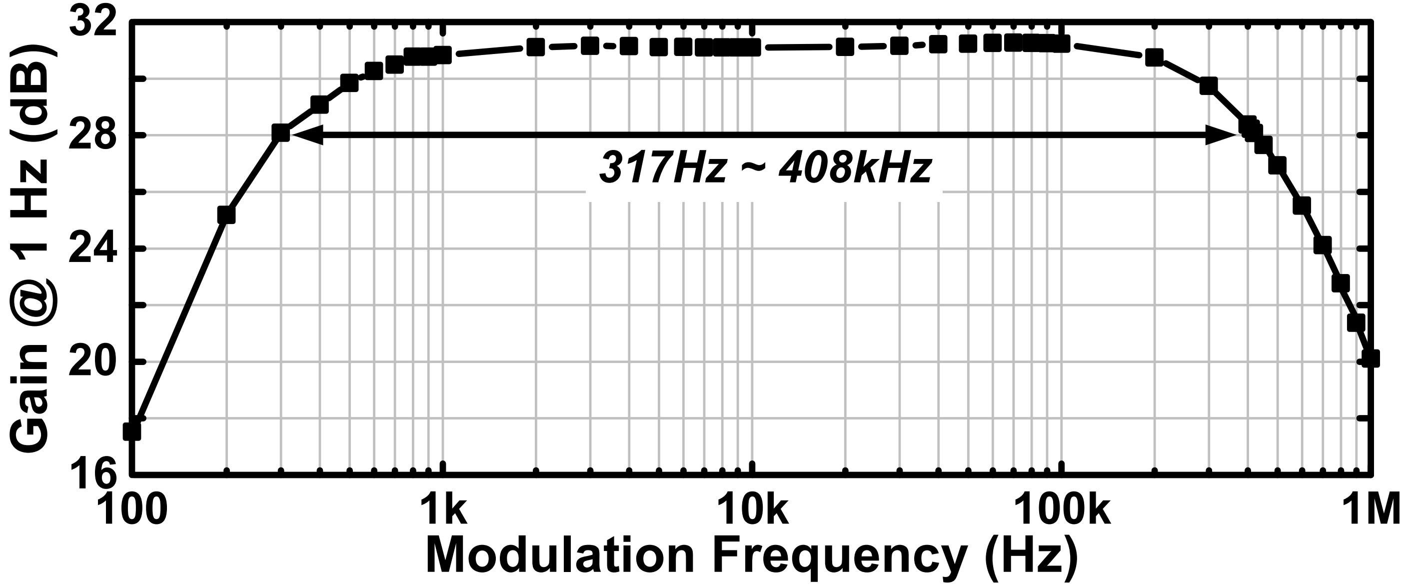


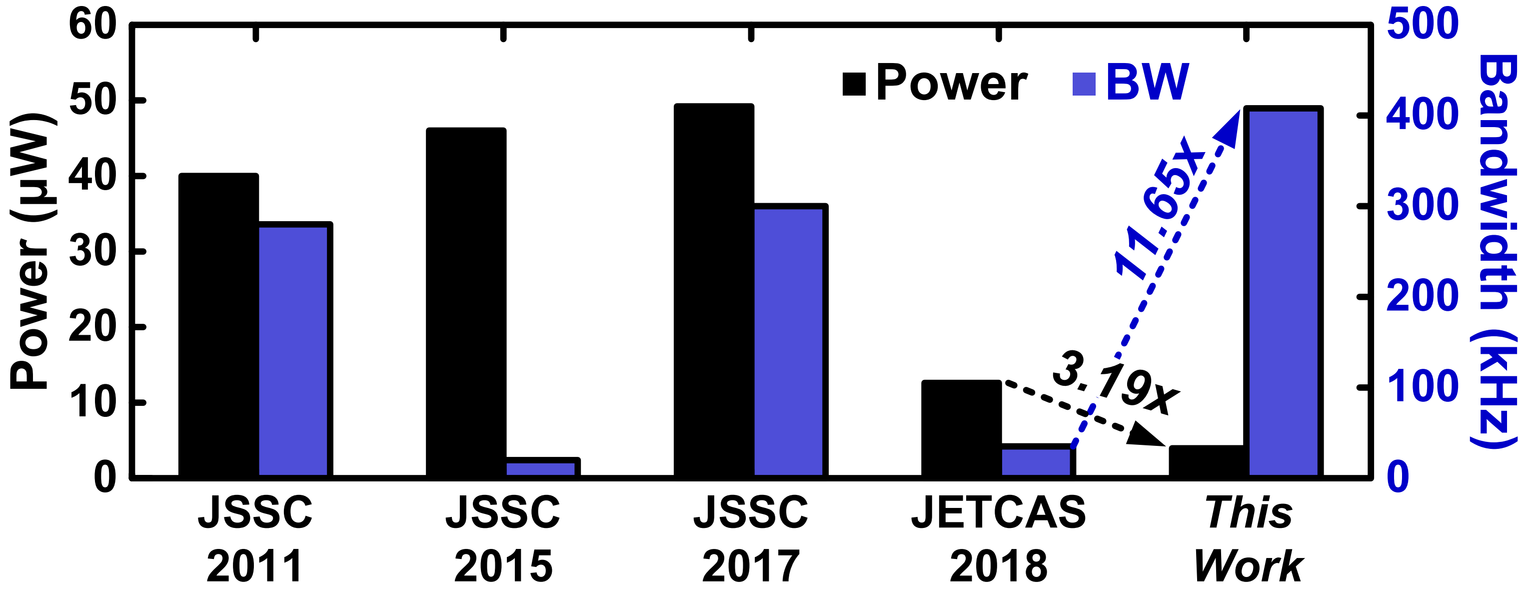




[1]K. Kim, ISSCC 2019 + JSSC 2020

# Power-BW-Efficient Amplifier[1]

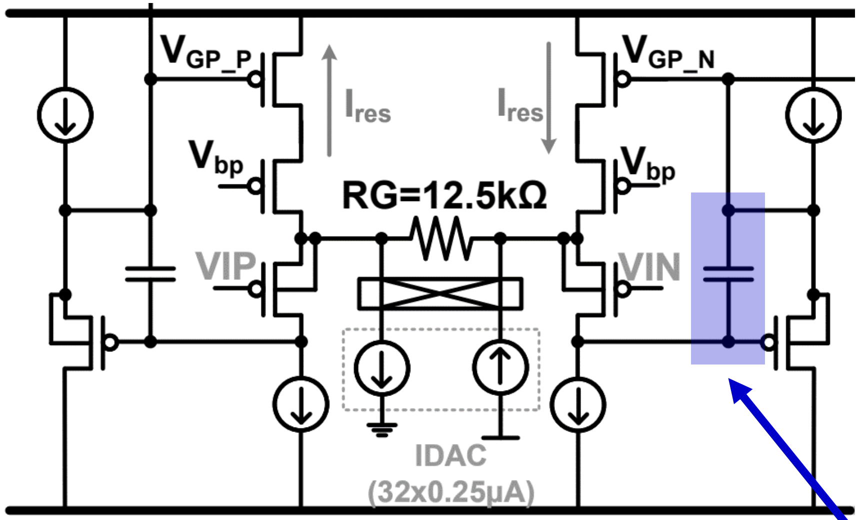


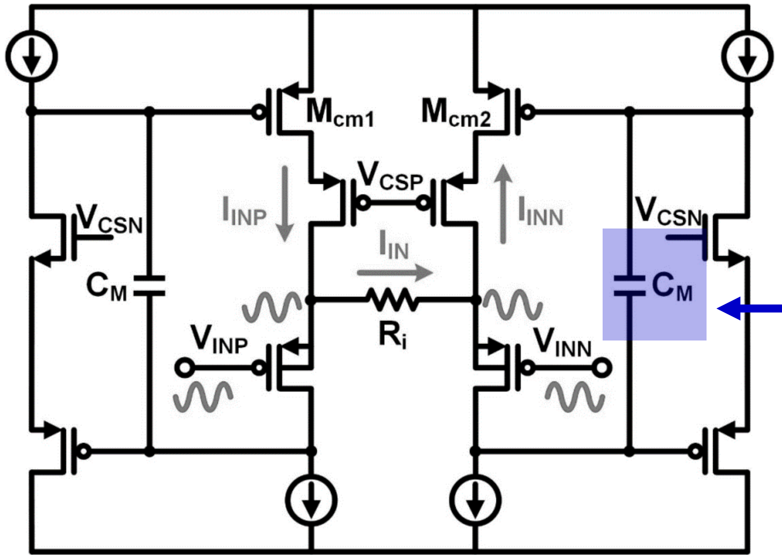

[1]K. Kim, ISSCC 2019 + JSSC 2020

# Adoption in Other Works

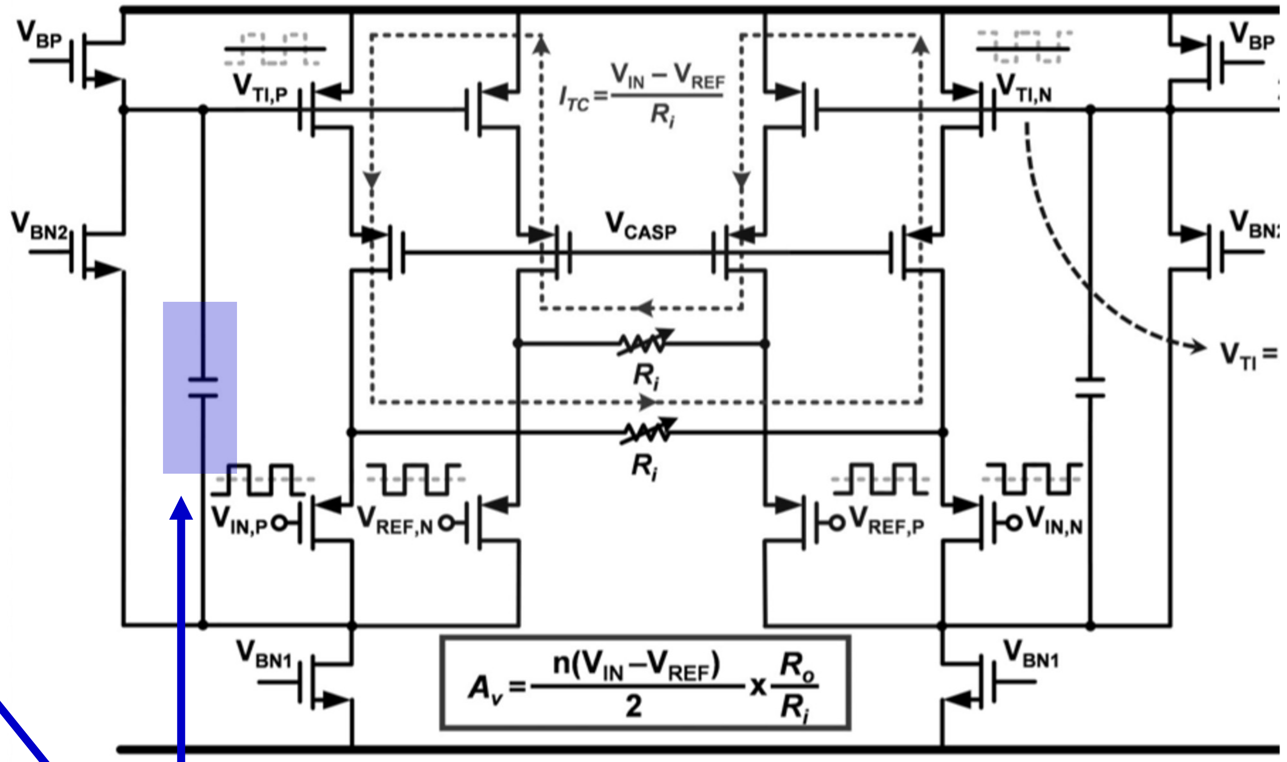
T. Zhang, ISSCC 2021 (A*STAR)




Q. Pan, ISSCC 2022 (Fudan Univ.)




S.-I. Cheon, ISSCC 2024 (KAIST)




**Lead Compensated** buffer design has been **Widely Adopted!**

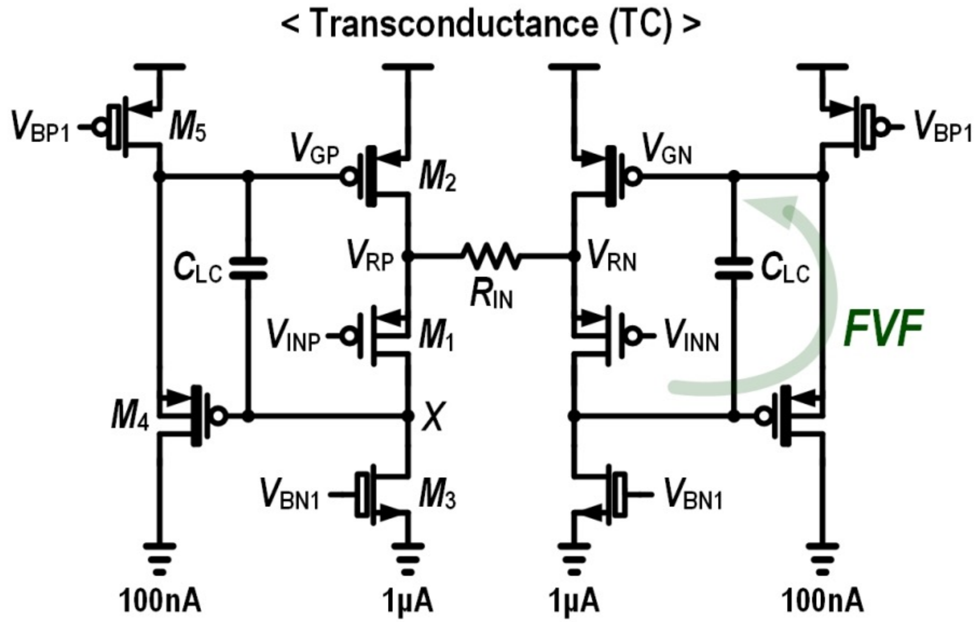
# *Open-Sourced* Amplifier Design[1]

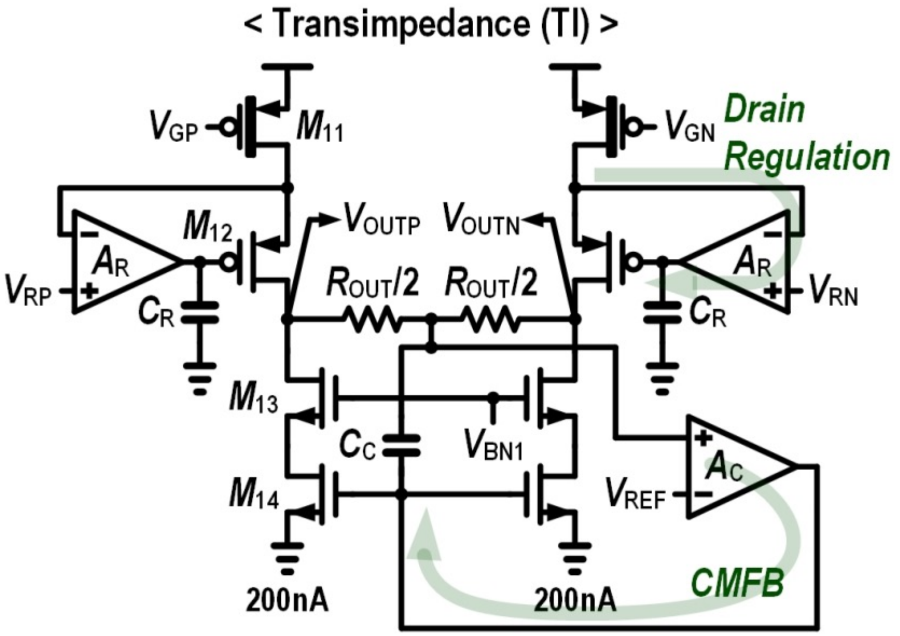
A 3.11 $\mu$W 40 nV/$\sqrt{}$Hz Instrumentation Amplifier for Bio-Impedance Sensors Exploiting Positive-Feedback-Assisted Gain Boosting

Kwantae Kim and Shih-Chii Liu
Institute of Neuroinformatics, University of Zürich and ETH Zürich, 8057 Zürich, Switzerland
Email: {kwantae, shih}@ini.uzh.ch

TABLE I
DESIGN PARAMETERS OF THE BASELINE IA

| TC Stage | $W/L$ ($\mu$m) | $A_R$ Amplifier | $W/L$ ($\mu$m) |
|---|---|---|---|
| $M_1$ | 500/0.25 | $M_{R1}$ | 0.25/0.25 |
| $M_2$ | 5×(0.5/4) | $M_{R2}$ | 0.25/0.25 |
| $M_3$ | 5/16 | $M_{R3}$ | 0.25/0.25 |
| $M_4$ | 1/0.25 | $M_{R4}$ | 0.5/16 |
| $M_5$ | 0.25/4 | $C_R$ | 5 fF |
| $C_{LC}$ | 100 fF | | |
| **TI Stage** | **$W/L$ ($\mu$m)** | **$A_C$ Amplifier** | **$W/L$ ($\mu$m)** |
| $M_{11}$ | 0.5/4 | $M_{C1}$ | 0.25/0.25 |
| $M_{12}$ | 1/0.25 | $M_{C2}$ | 0.25/0.25 |
| $M_{13}$ | 0.5/0.5 | $M_{C3}$ | 0.25/0.25 |
| $M_{14}$ | 0.25/16 | $M_{C4}$ | 0.25/4 |
| $C_C$ | 100 fF | $V_{REF}$ | 0.5 V |
| $R_{OUT}$ | 500×$R_{IN}$ | | |

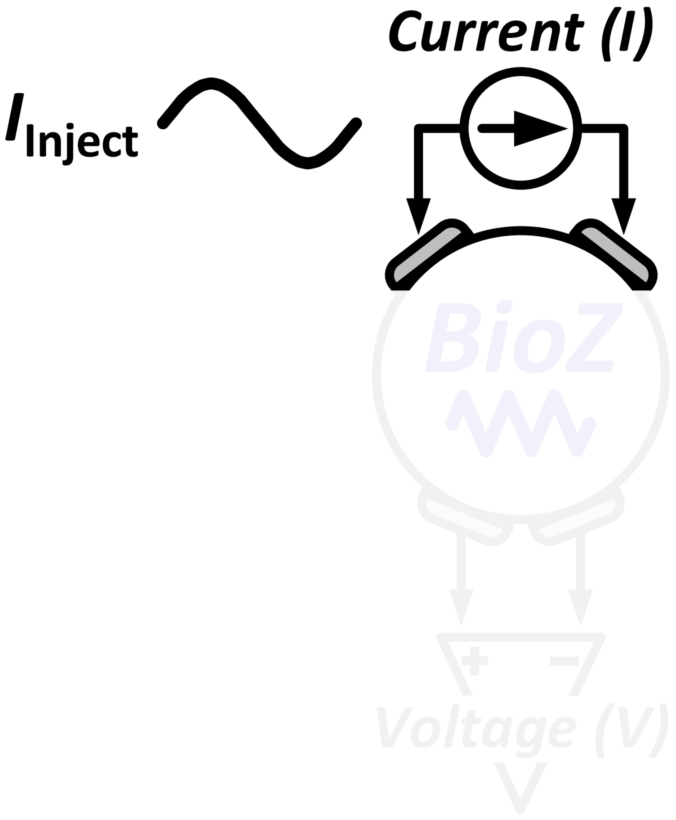


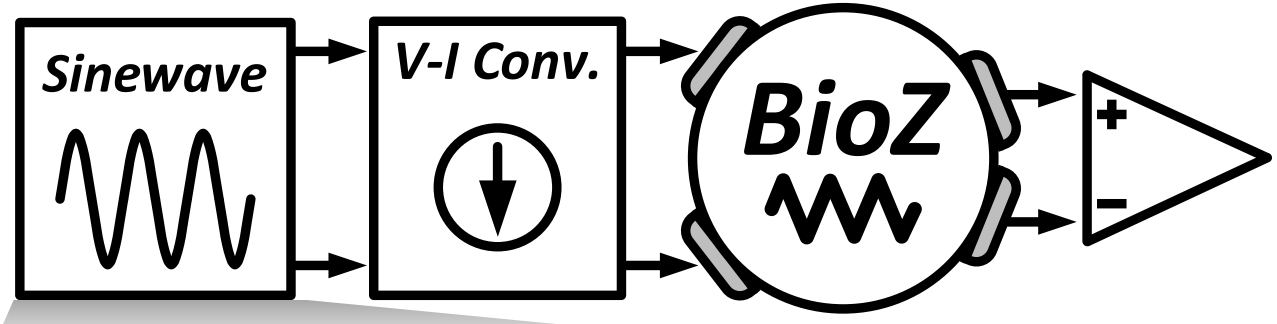

*Open-Sourced*
**Schematic Parameters (TSMC 65nm)**

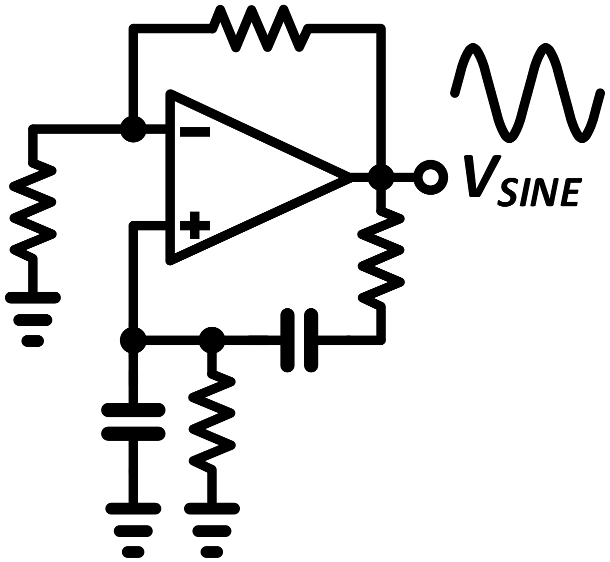
# Bioimpedance (BioZ) Sensing

$$\text{BioZ} = \frac{V_{\text{Sense}}}{I_{\text{Inject}}}$$

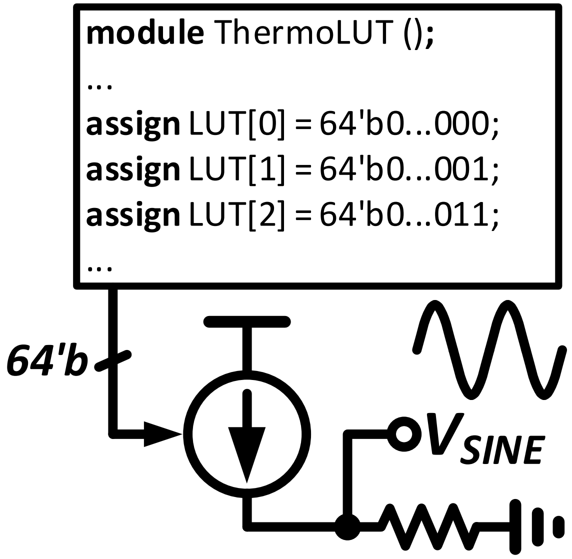


# Sinewave Generation



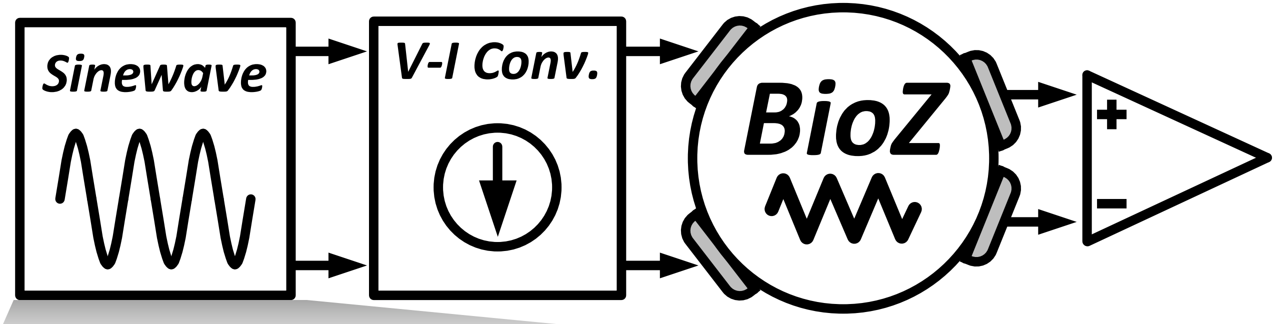

**Analog RC-OSC[1]**



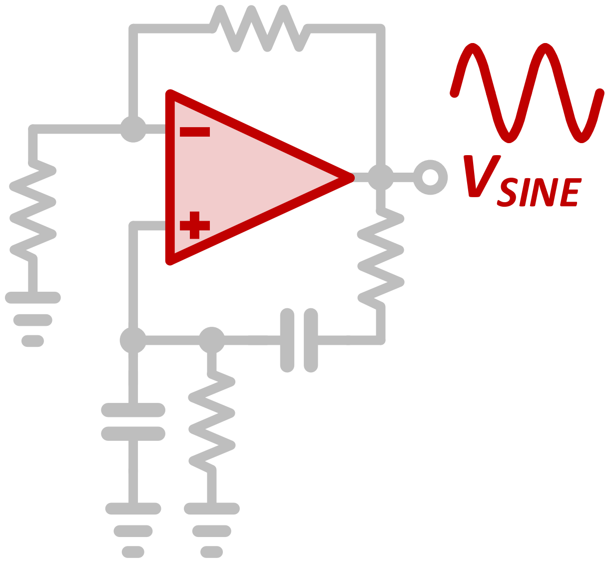

**Digital LUT + Analog DAC[2]**

[1]S. Hong, ISSCC 2014 [2]M. Kim, ISSCC 2017

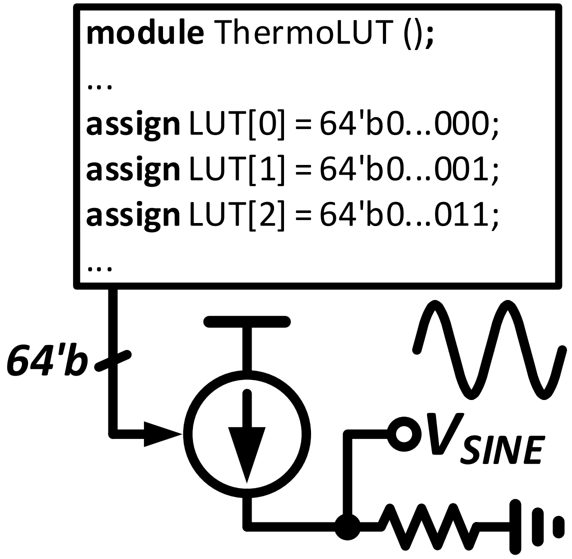
# Sinewave Generation




☹ >100μW



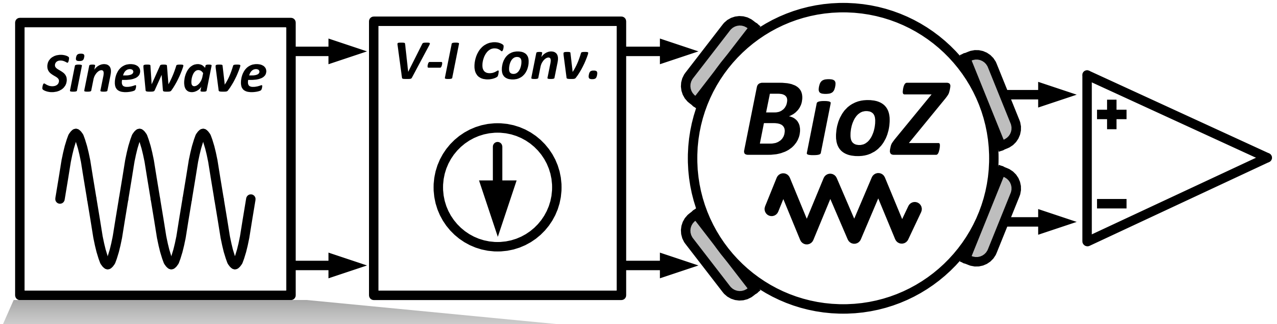

Analog RC-OSC[1]



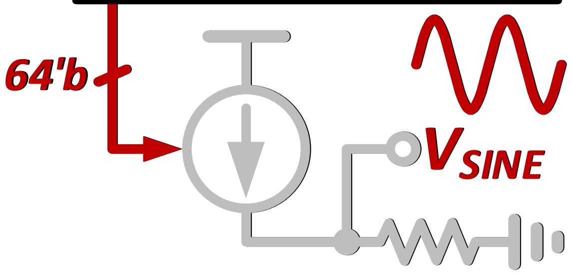

Digital LUT
+ Analog DAC[2]

[1]S. Hong, ISSCC 2014 [2]M. Kim, ISSCC 2017

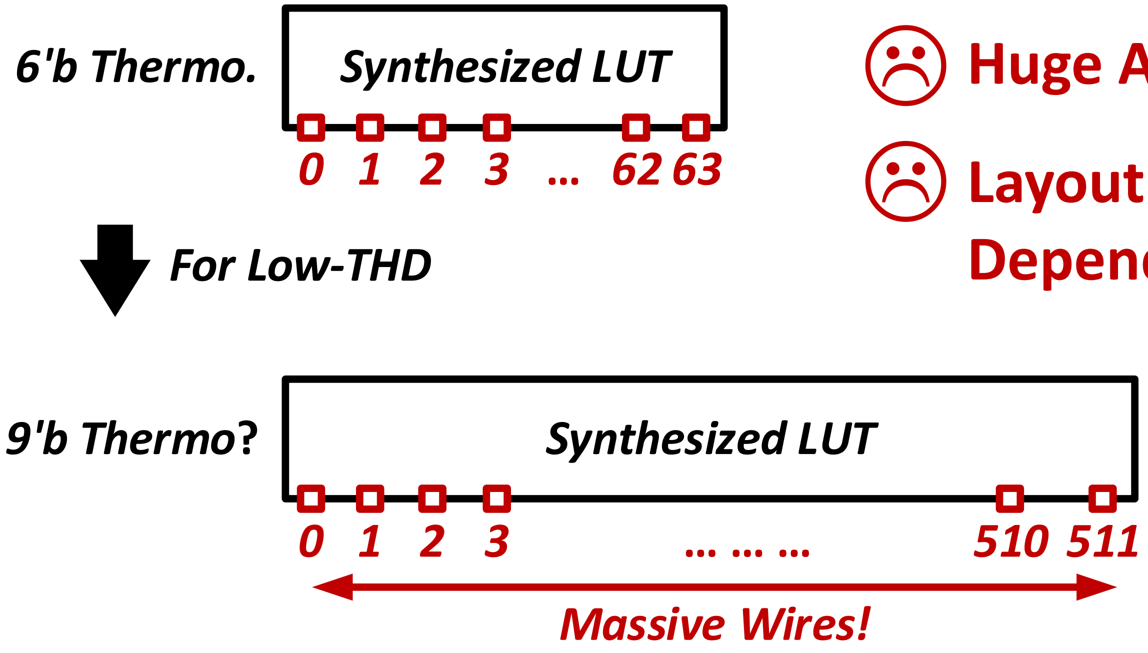
# Sinewave Generation




```
module ThermoLUT ();
...
assign LUT[0] = 64'b0...000;
assign LUT[1] = 64'b0...001;
assign LUT[2] = 64'b0...011;
...
```




Digital LUT
+ Analog DAC[2]



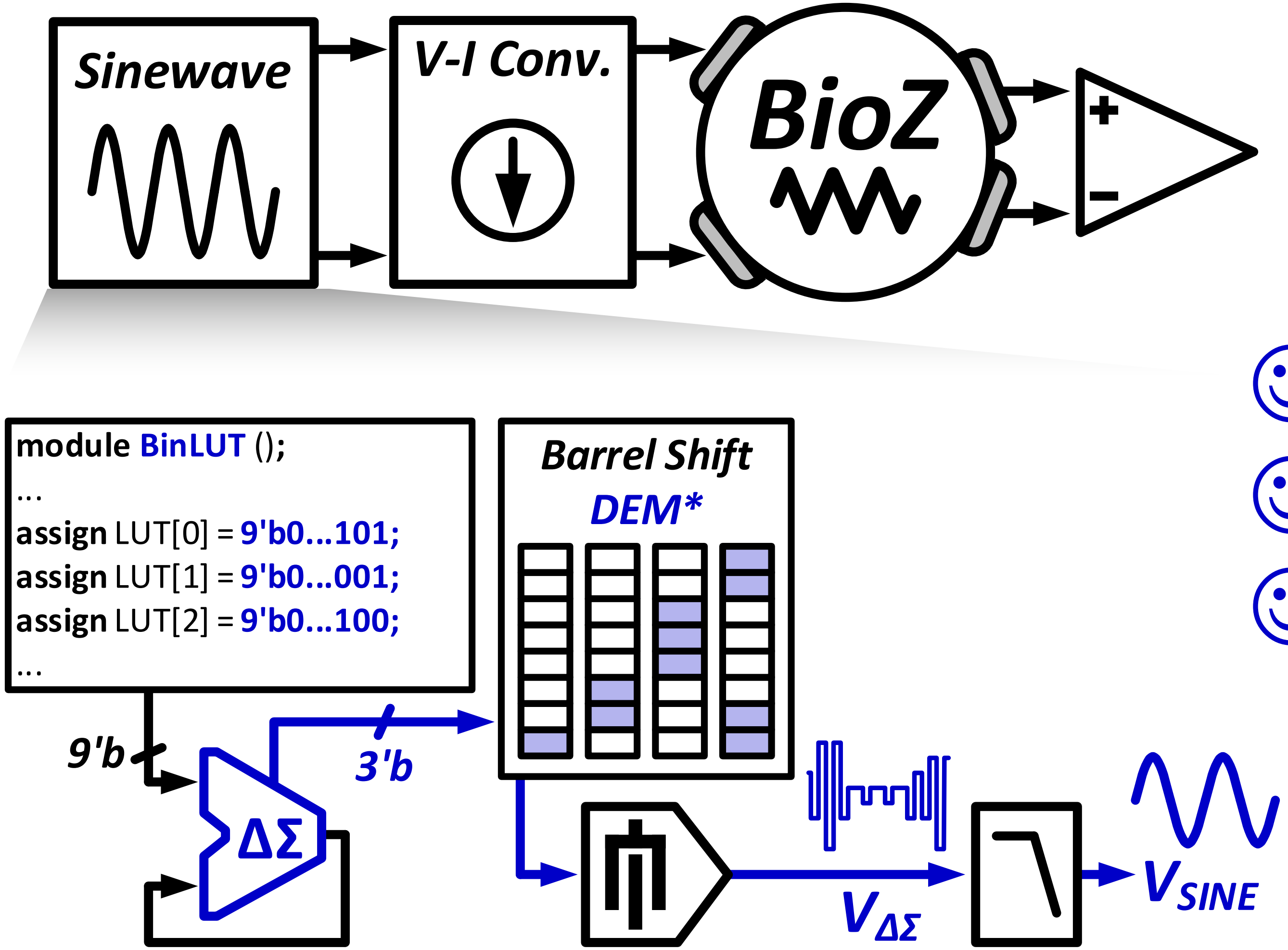

☹ Limited THD

☹ Huge Area

☹ Layout Quality Dependency

[2]M. Kim, ISSCC 2017

# Digital ΔΣ[1] Sinewave Generation



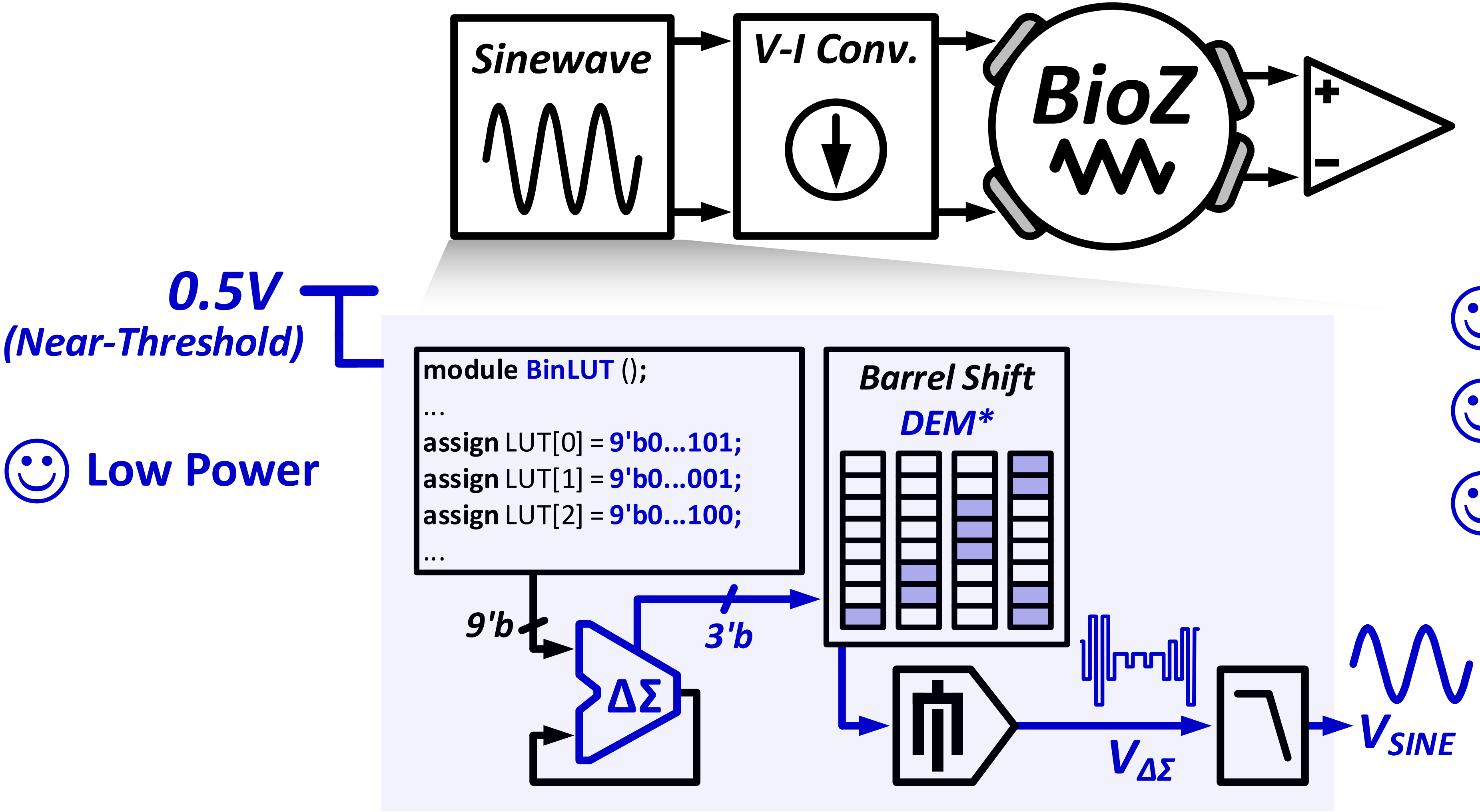

- ☺ Low THD
- ☺ Compact Area
- ☺ Layout Quality Independent (DEM)

**Digital LUT + Digital ΔΣ + Analog DAC + Analog LPF**

[1]K. Kim, VLSI 2020 + JSSC 2022

*Dynamic Element Matching (DEM)

# Digital ΔΣ[1] Sinewave Generation




☺ Low Power

☺ Low THD

☺ Compact Area

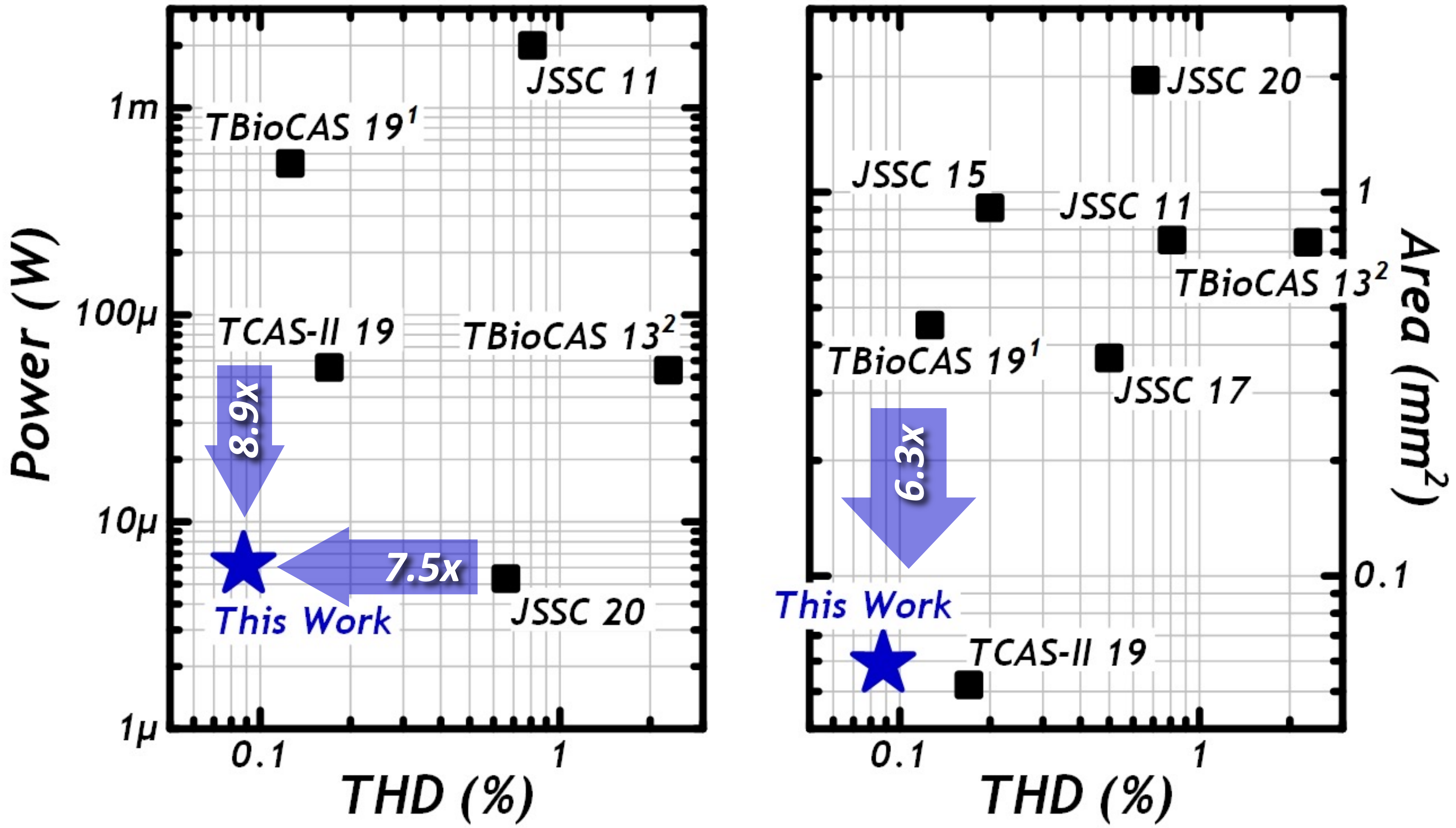
☺ Layout Quality Independent (DEM)

**Digital LUT + Digital ΔΣ + Analog DAC + Analog LPF**

[1]K. Kim, VLSI 2020 + JSSC 2022

*Dynamic Element Matching (DEM)

# Comparison Graph




**The First Sub-10μW, Sub-0.1% THD**
**Sinusoidal Current Generator for BioZ Sensor ICs**

[1]K. Kim, VLSI 2020 + JSSC 2022

# *Open-Sourced* Sinewave Generator[1,2]

박 사 학 위 논 문
Ph.D. Dissertation

정확한 위상 측정이 가능한 저전력
생체임피던스 센서 회로

Low Power Bio-Impedance Sensor IC
with Precise Phase Measurement

2021

김 관 태 (金 官 泰 Kim, Kwantae)

한 국 과 학 기 술 원

Korea Advanced Institute of Science and Technology

the 2nd-order LPF which follows the capacitive-DAC as depicted in Figure 31. In addition, a doubled sampling ratio from 64× to 128× helps to relax the filter design requirements. Finally, when it is 3rd-order ΔΣ modulated, the output spectrum looks like rightmost graph of Figure 34. With the 20 kHz of output frequency, we can expect the overall noise sources, including spurs and quantization noise, can be suppressed down below the -60 dBc, after lo…

**MATLAB (Software)**

Alghouth similar concept of this approach was provided in [35], it required a large-bit-width of 18 bit in PRNG to dither its poor spur performance of the oscillator, degrading its power efficiency. Here, the most of spur reduction is obtained only by the 9 bit LUT that is sufficient to provide > 70dB of in-band spur. Furthermore, the use of error-feedback-based ΔΣ modulator halves the required number of accumulators in each of the modulator stages compared to the output-feedback structure [35], greatly simplifying the implementation of the ΔΣ modulator.

The integer-numbered sinewave is generated using MATLAB environment. Detailed MATLAB code is provided as below.

**Table II. MATLAB Code Used for the Generation of Pseudo-Sine Waveform**

```
%% Start
% Created by Kwantae Kim, 2019
clc;
clear;
close all;

% Global Parameters
clock=2.56*10^6;
OSR=128;

%% PseudoSine Parameters
Am = OSR*2;          % Define Amplitude for the Integer Components of LUT
                     % This is not a Pk-Pk value
f = clock/OSR;       % Frequency
AmHigh = Am-1;       % Max. Amplitude
AmLow = -Am+1;       % Min. Amplitude

%% Array Generation (Sine, PseudoSine)
t=1/(f*OSR) : 1/(f*OSR) : (1/f);     % x-axis for Time (1 Period)
Sine=AmHigh*sin(2*pi*f*t);           % Sine Generation

PseudoSineValue = zeros(1,OSR);      % Array for PseudoSine Value
PseudoSineValue(1) = AmLow;
for i = 2:1:Am*2
    PseudoSineValue(i) = PseudoSineValue(i-1)+1;
end
```

4.2.2 Implementation of the Digital Circuit

Functional verifications of the register transfer level (RTL) design for the digital part of proposed CG IC is done with Cadence Virtuoso (AMS simulator), and the logic synthesis of RTL design is processed with Synopsys Design Compiler.

**Verilog (Hardware)**

Tab… …5 describes an instantiation-tree of the RTL design.

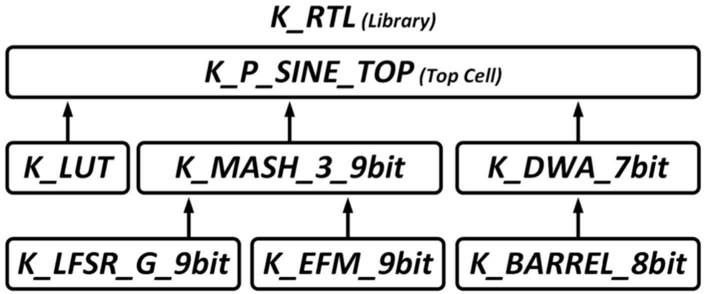



**Figure 35. Instantiation-tree of the RTL design.**

**Table III. Register Transfer Level Design of the Digital Part**

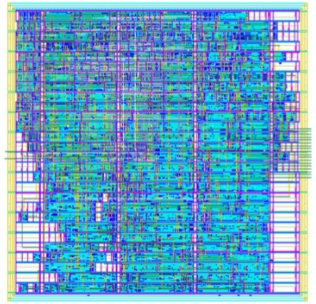
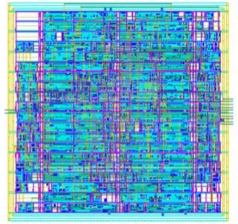
```
//Verilog HDL for "K_RTL", "K_P_SINE_TOP" "functional"

module K_P_SINE_TOP (
        input wire      clk,
        input wire      resetn,
        output wire     [7:0] sine_outp,
        output wire     [7:0] sine_outn,
        output wire     sine_dac_rst_p,
        output wire     sine_dac_rst_n
);

wire [8:0] lut_out;
K_LUT
lut(
        .clk      (clk),
        .resetn   (resetn),
        .out      (lut_out)
);

wire [6:0] dsm_out;
```

- 54 -

[1]K. Kim, VLSI 2020 + JSSC 2022    [2]K. Kim, Ph.D. Dissertation

# Adoption in Other Work

TABLE II
COMPARISON AND SUMMARY OF SSG PRESENTED IN [9] AND THIS BRIEF

| | SSG based on [9] | This work |
|---|---|---|
| |  |  |
| SFDR | 64.7 dBc | 64.6 dBc |
| THD | 0.089% | 0.074% |
| Output | 3 bits | 2 bits |
| Power[a] | 44.7 $\mu$W | 24.8 $\mu$W |
| Cell area[b] | 10148 $\mu m^2$ | 5334 $\mu m^2$ |
| Floorplan area[b,c] | 13447 $\mu m^2$ | 7252 $\mu m^2$ |

[a] $V_{DD} = 1.8$ V, $f_{CK} = 4$ MHz,
[a,b] Using the same 0.18 $\mu$m CMOS standard cells,
[c] Layout that meets DRC requirements and is fully routed.

1764 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 70, NO. 5, MAY 2023

## A Sinusoidal Signal Generator Using a Delta-Sigma Modulated Look-Up Table and Analysis of Dither

Jaehyeong Park, *Graduate Student Member, IEEE*, and Matthew L. Johnston, *Senior Member, IEEE*

[9] K. Kim, S. Kim, and H.-J. Yoo, "Design of sub-10-$\mu$W sub-0.1% THD sinusoidal current generator IC for bio-impedance sensing," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 586–595, Feb. 2022.

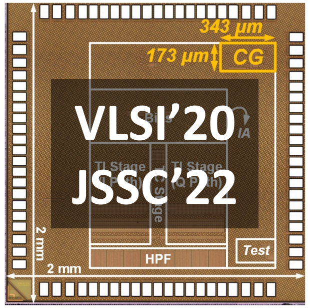
[14] K. Kim, "Low power bio-impedance sensor IC with precise phase measurement," Ph.D. dissertation, School Electr. Eng., Korea Adv. Inst. Sci. Technol., Daejeon, South Korea, 2021.

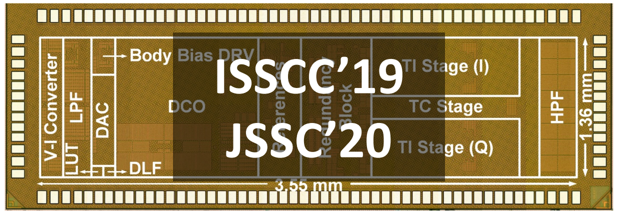
**The design is Replicated & Improved by Oregon State University**

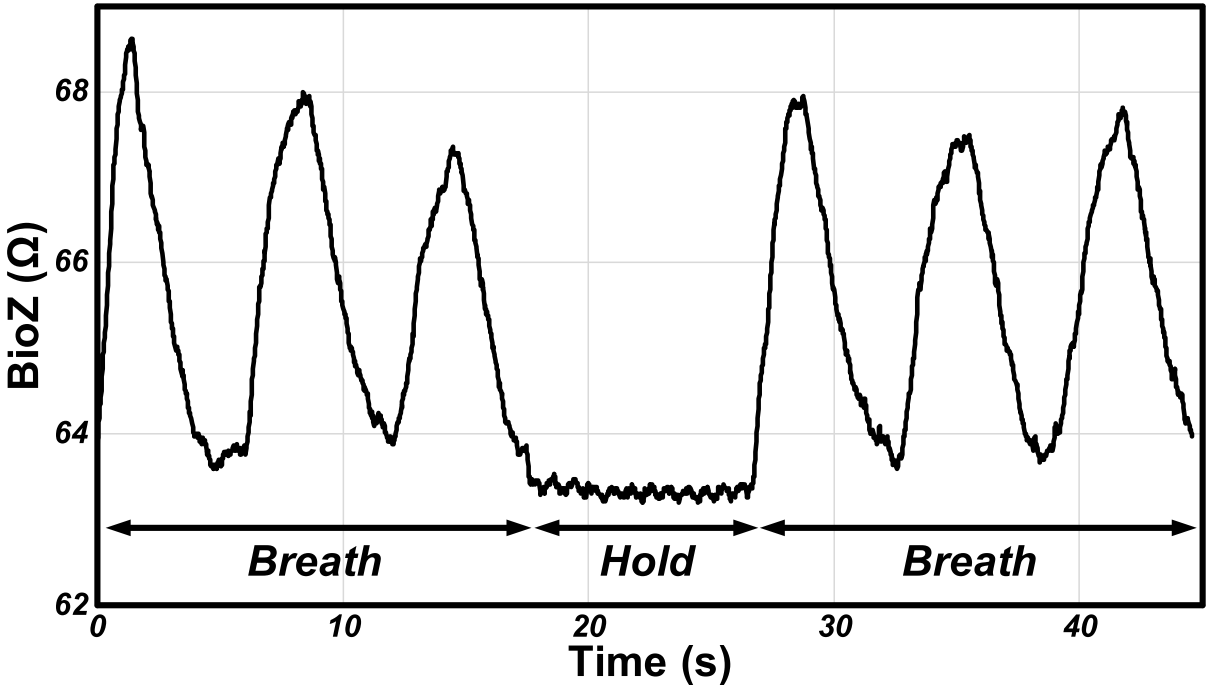
[1] J. Park, TCAS-II 2023

# In-Vivo BioZ Measurement

$$\text{BioZ} = \frac{V_{\text{Sense}}}{I_{\text{Inject}}}$$

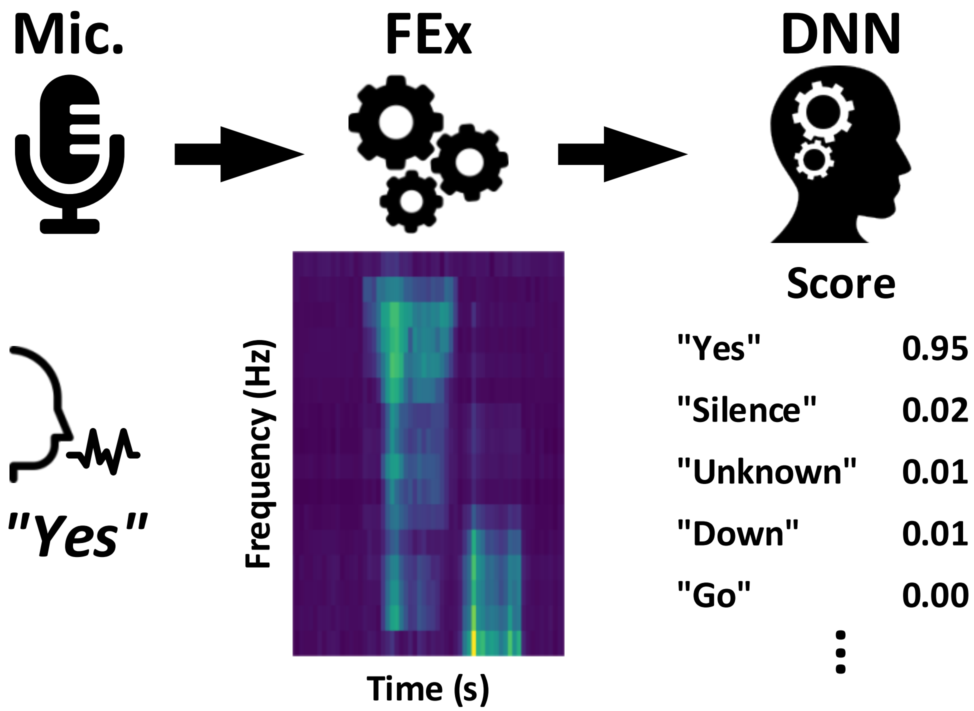
# Biomedical Sensor IC

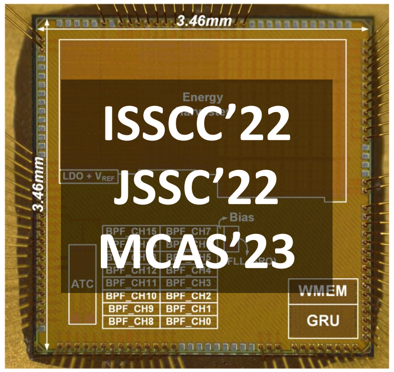




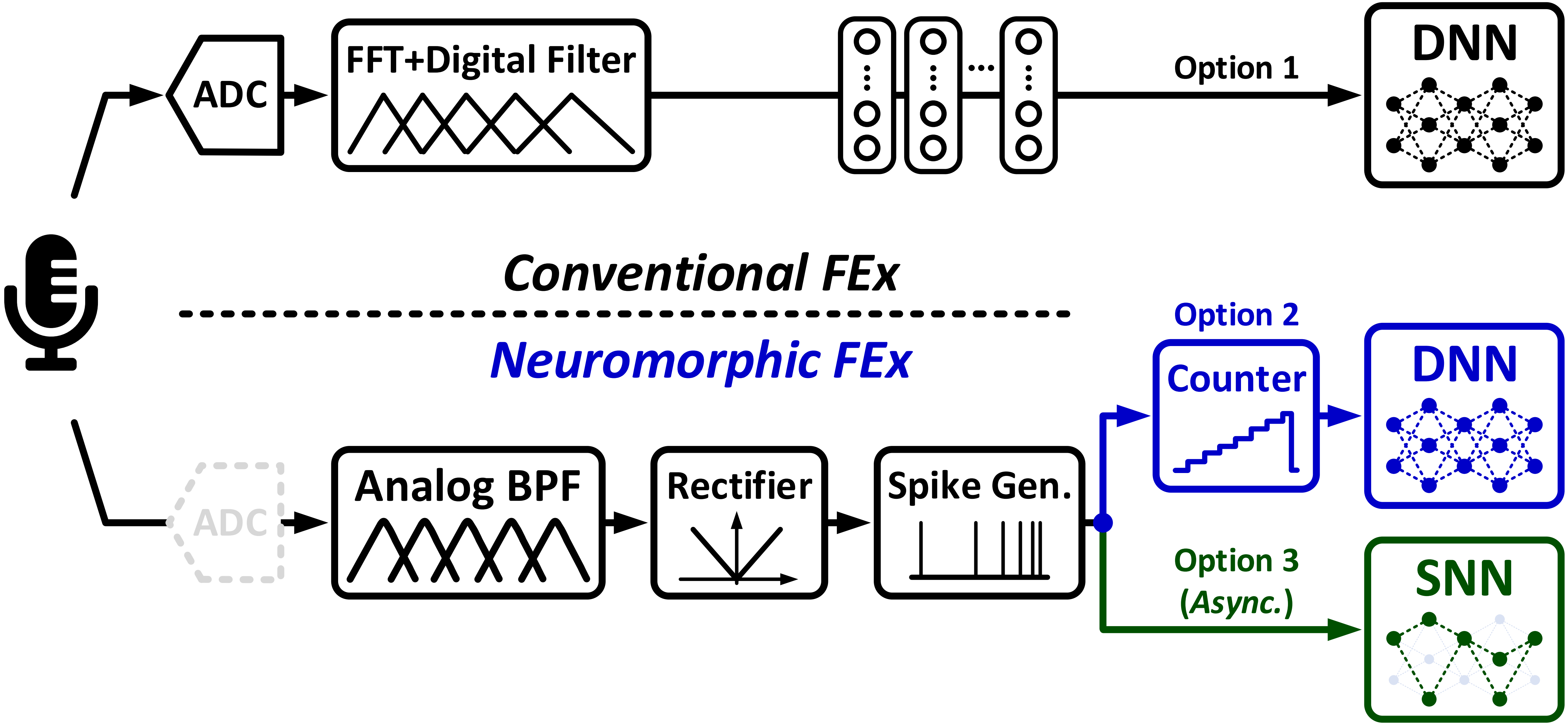


# Neuromorphic Sensor IC



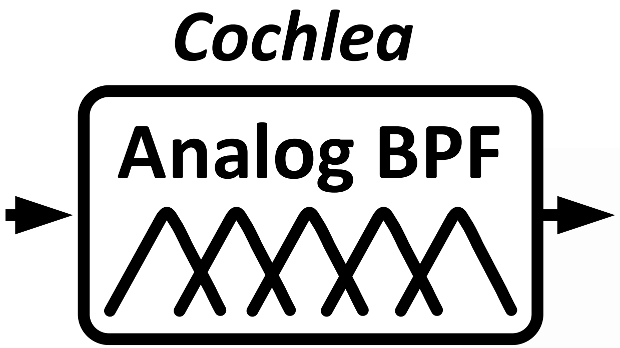



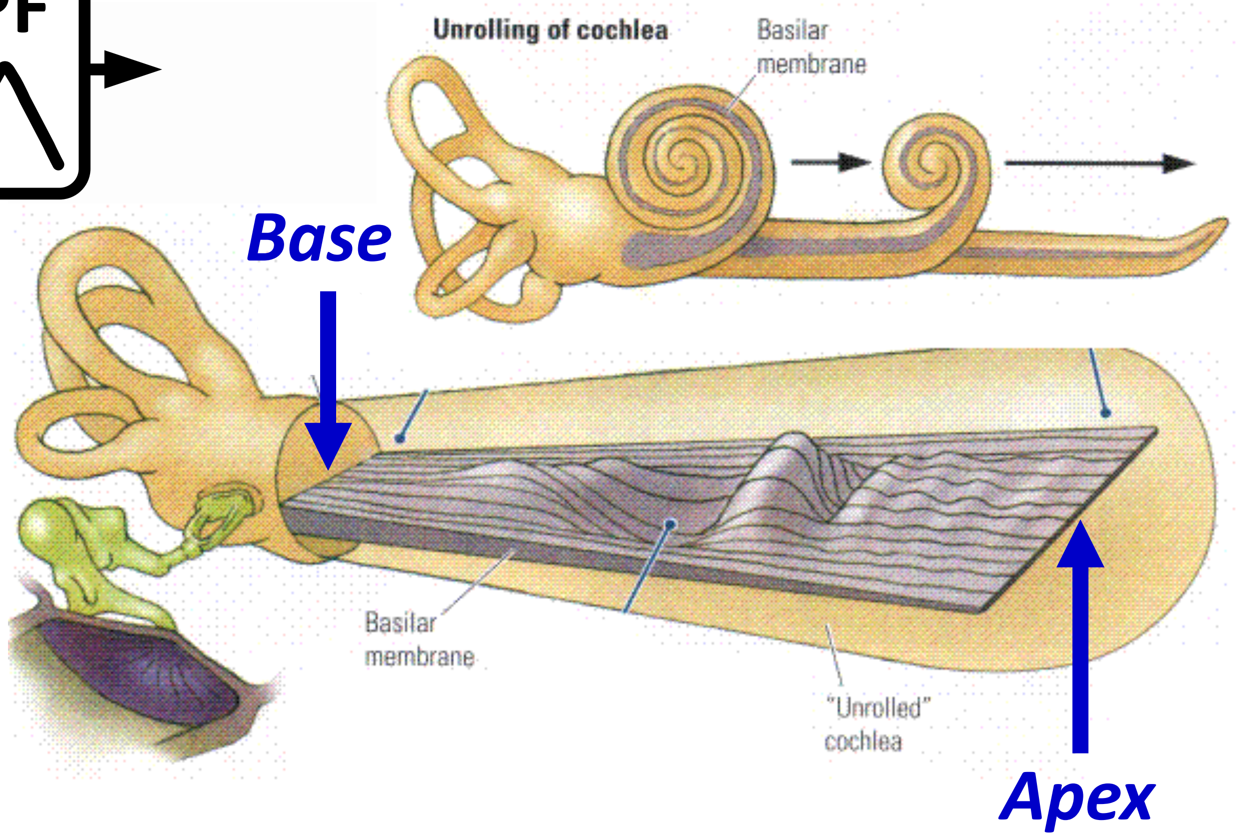
# Neuromorphic Audio Processing Architecture

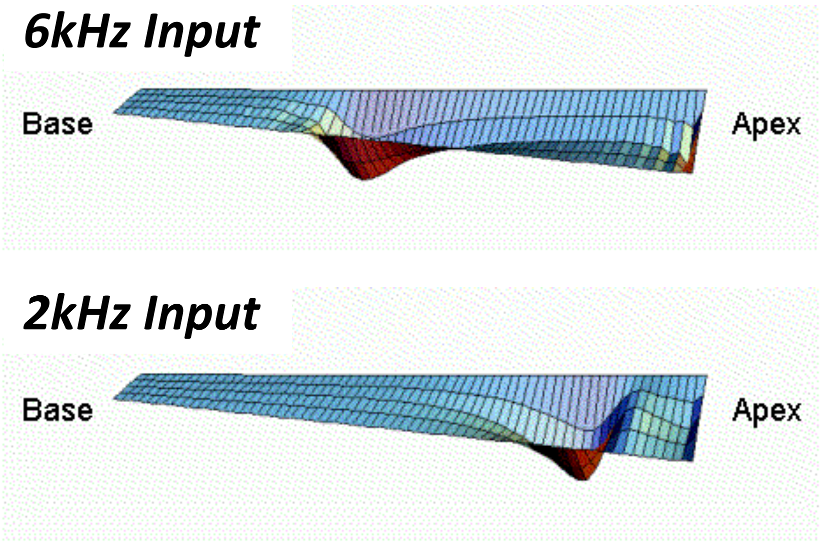



K. Kim, CAS Magazine 2023

# Neuromorphic Audio Processing Architecture



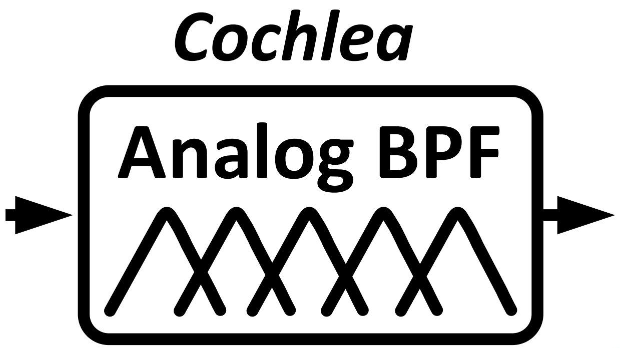



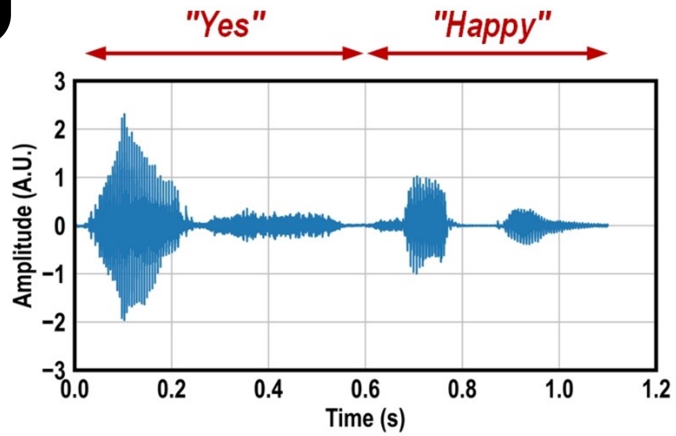



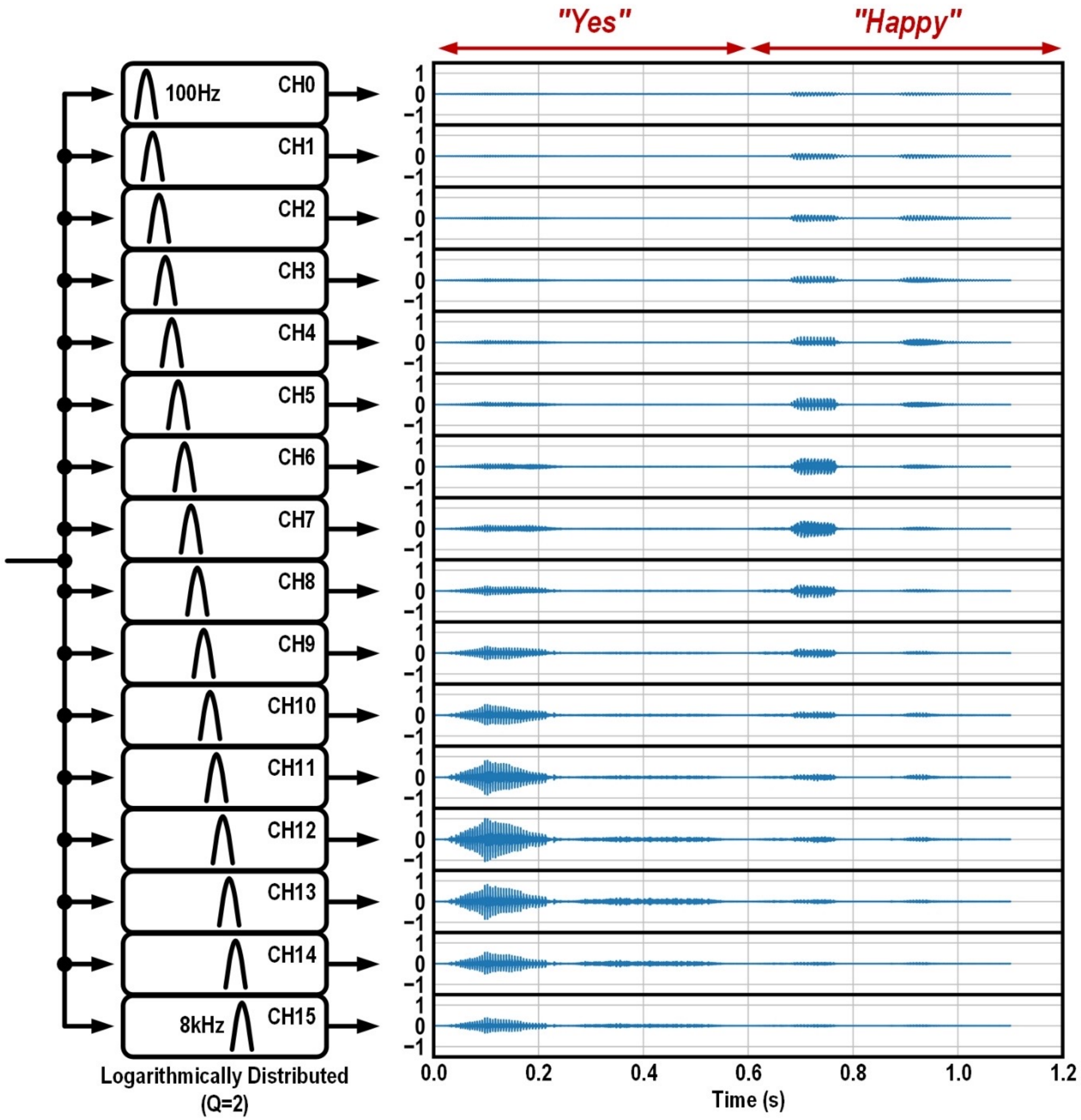

Kolb and Willshaw, 2001

Hiroshi Wada, Tohoku University

# Neuromorphic Audio Processing Architecture

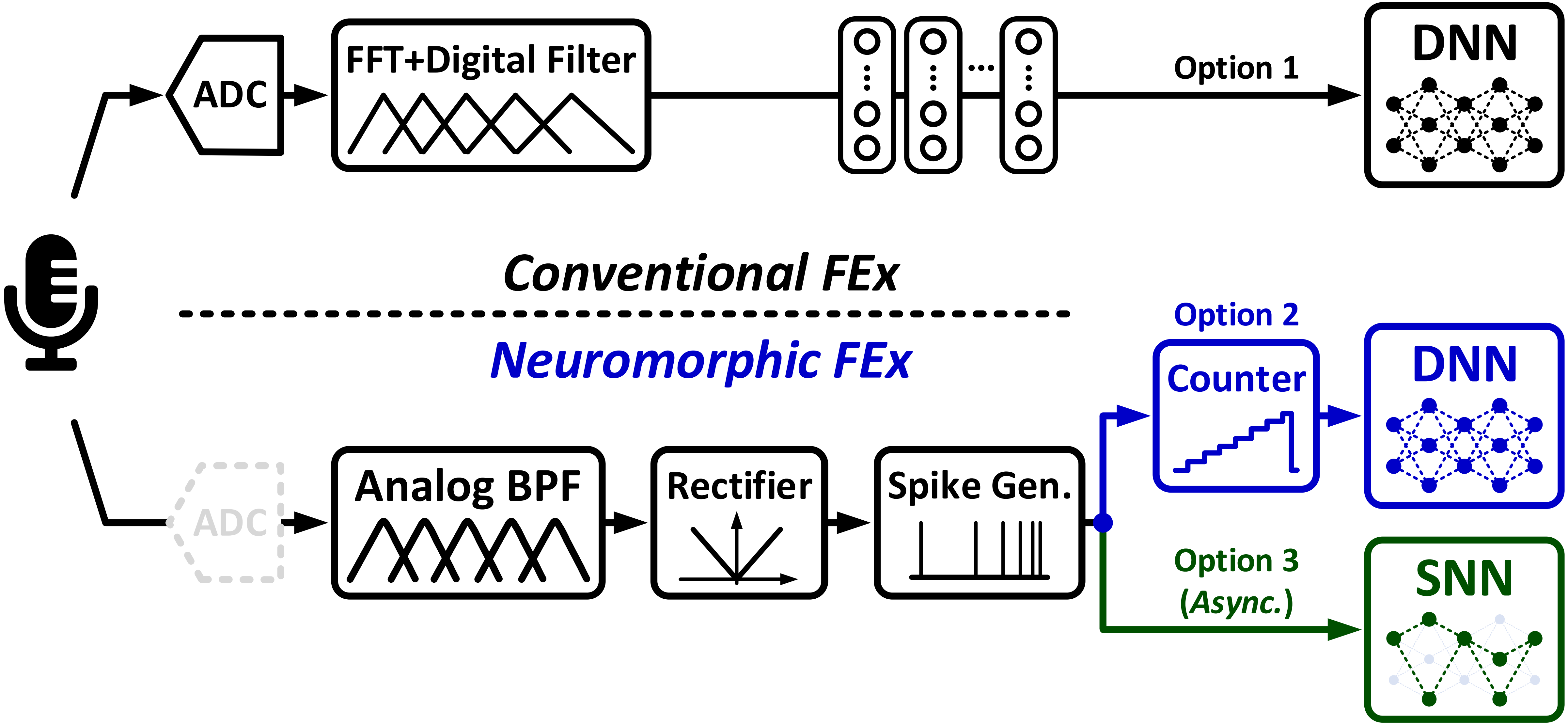


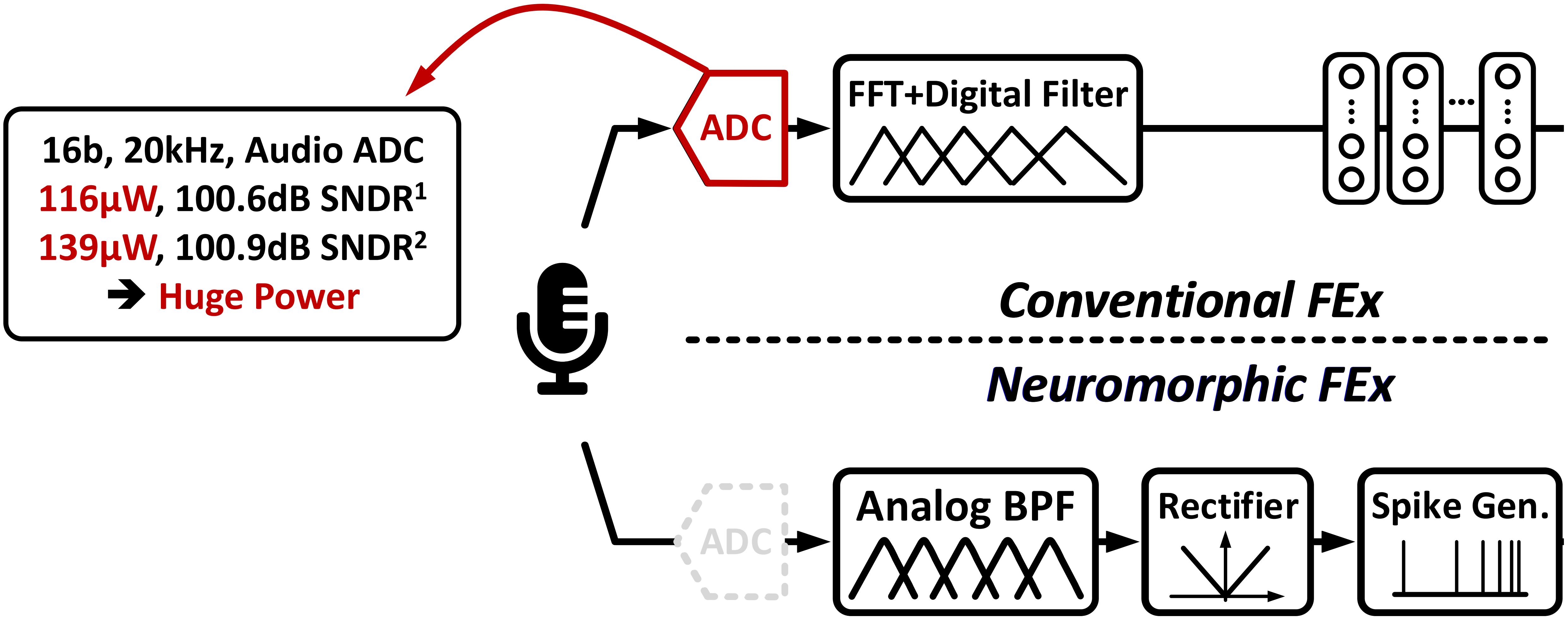

K. Kim, CAS Magazine 2023

# Neuromorphic Audio Processing Architecture




K. Kim, CAS Magazine 2023

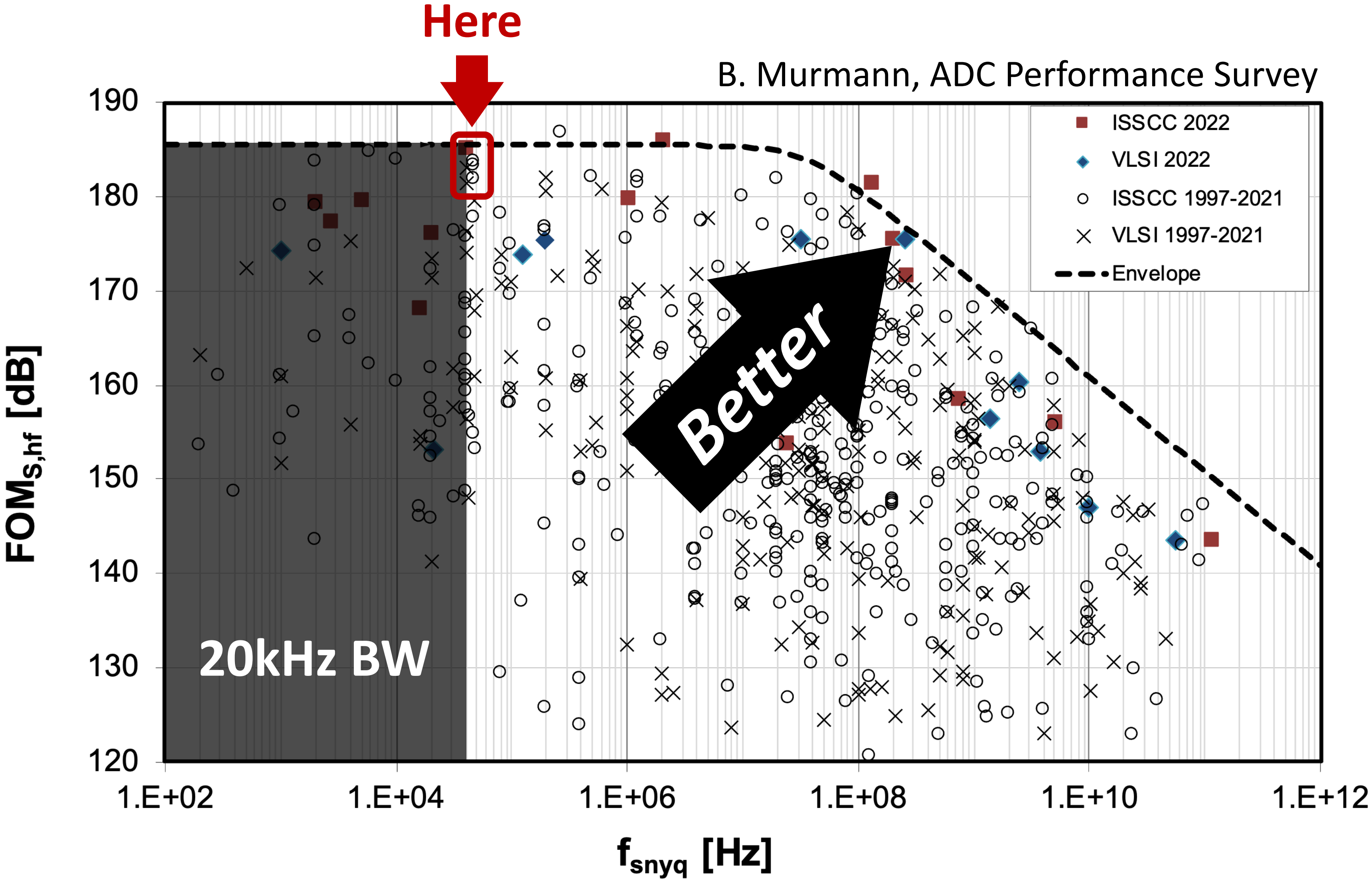
# Why Neuromorphic Approach? – 1. ADC




[1]C. Lo, ISSCC 2021 [2]S. Mondal, ISSCC 2021

# Why Neuromorphic Approach? – 1. ADC

16b, 20kHz, Audio ADC
116μW, 100.6dB SNDR[1]
139μW, 100.9dB SNDR[2]
➔ Huge Power




[1]C. Lo, ISSCC 2021
[2]S. Mondal, ISSCC 2021

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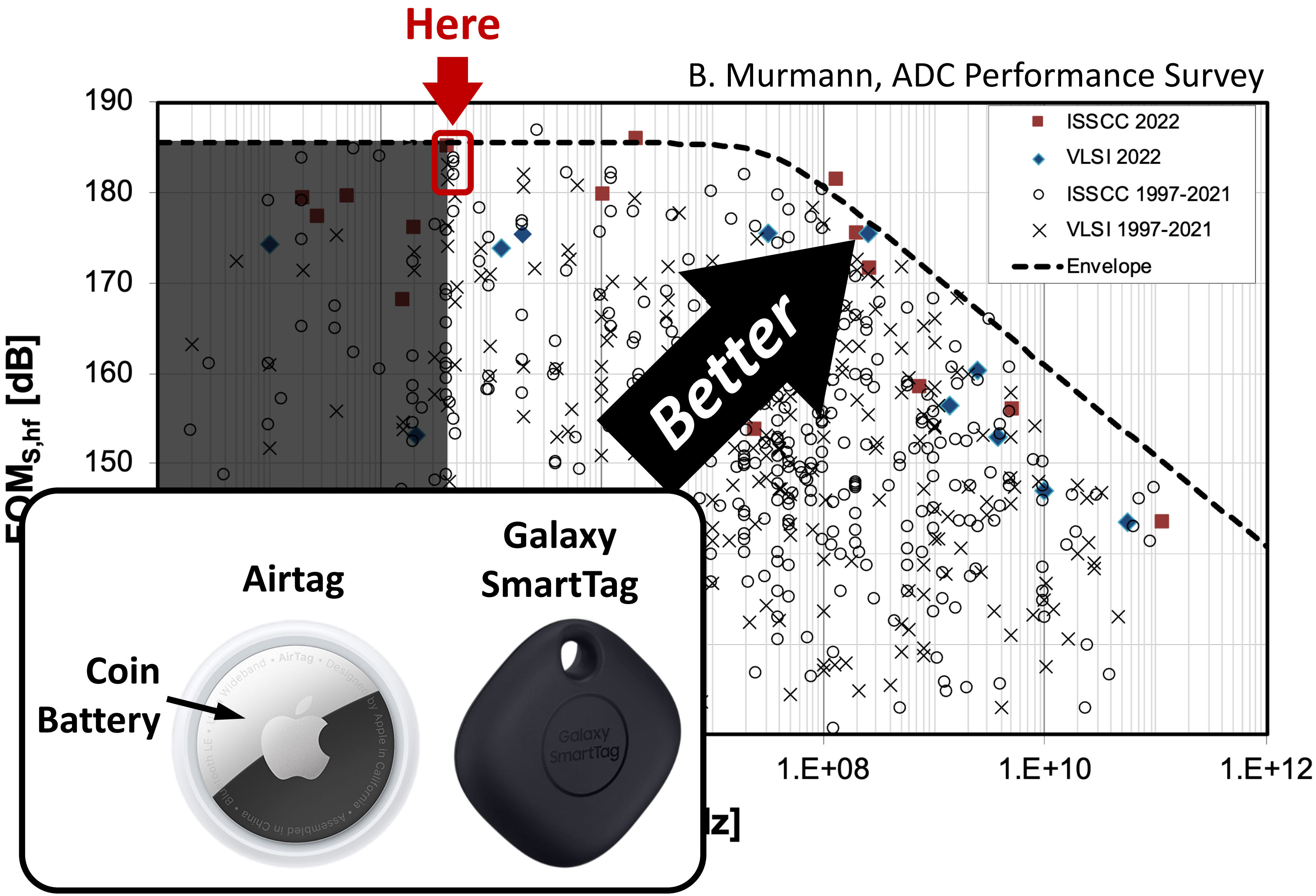
**System Bottleneck** for Always-On TinyML Devices!
(<1 Year Solely by ADC Power)




[1]C. Lo, ISSCC 2021 [2]S. Mondal, ISSCC 2021

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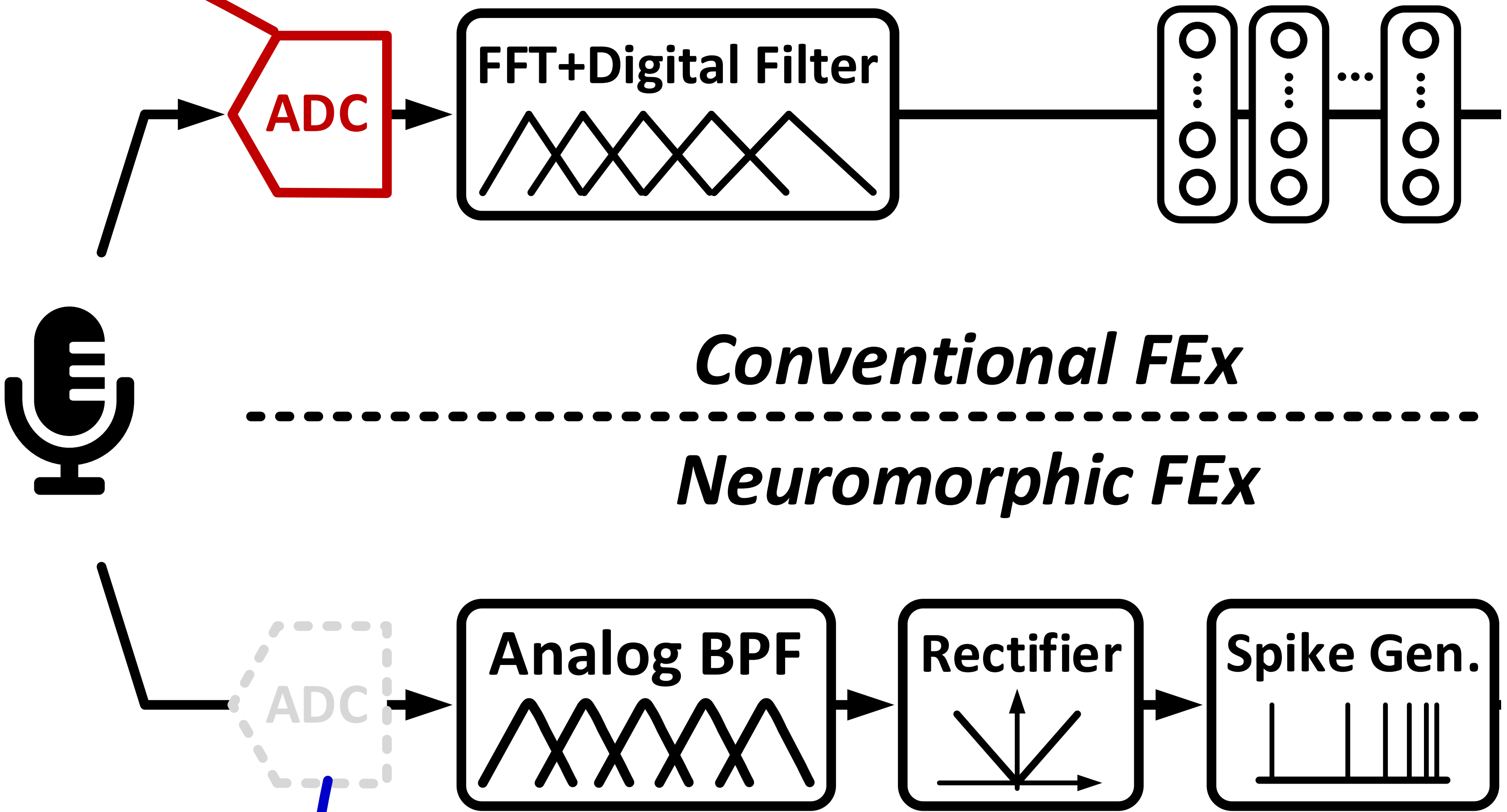
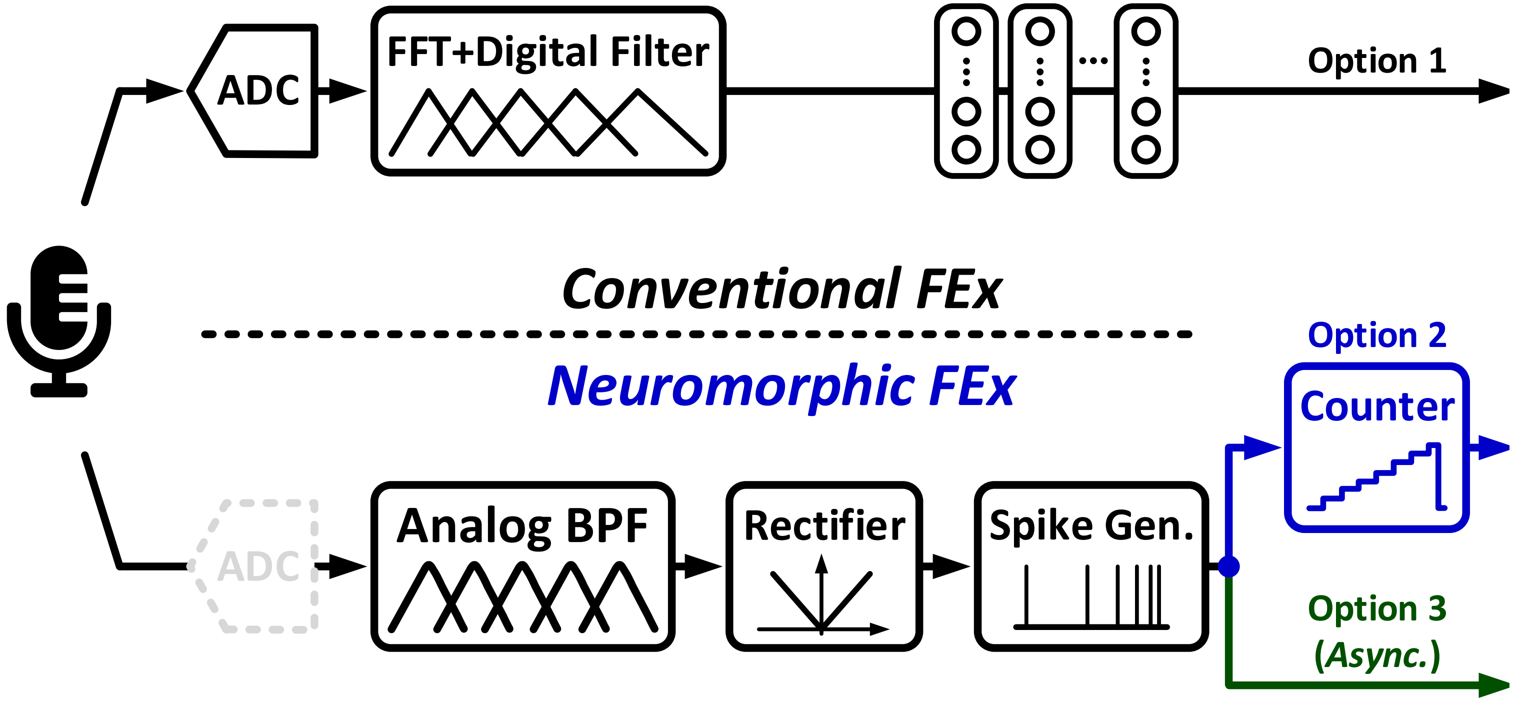
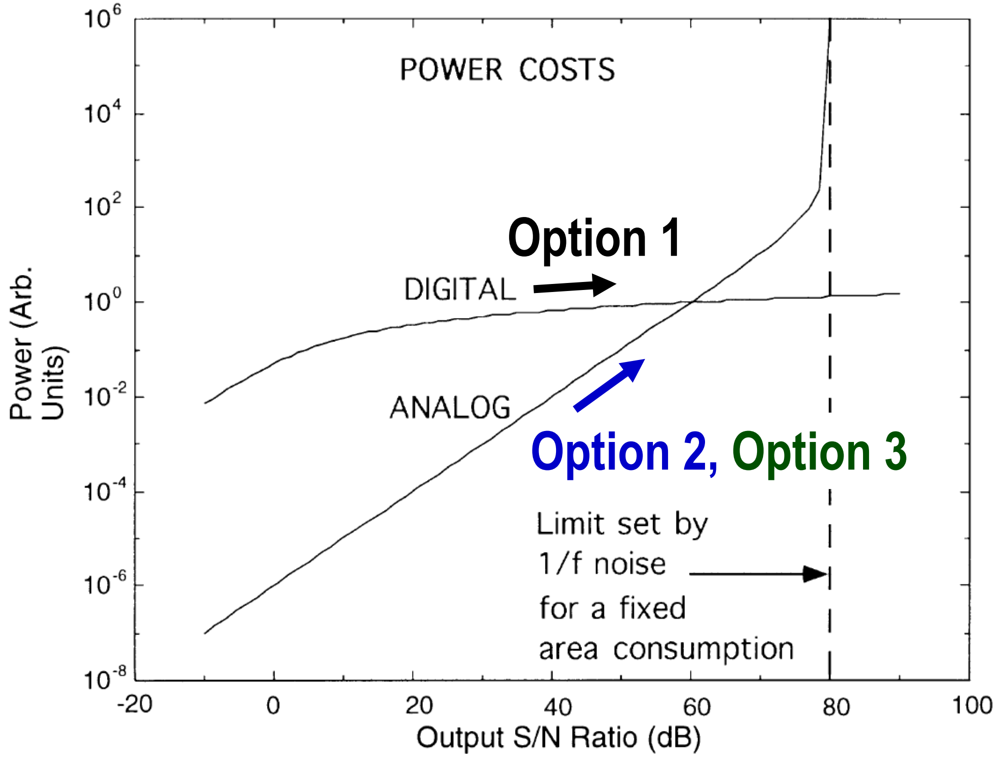



*Bypassing ADC* is a Breakthrough Towards *Ultra-Low-Power Operation*

[1]C. Lo, ISSCC 2021 [2]S. Mondal, ISSCC 2021

# Why Neuromorphic Approach? – 2. Analog vs Digital



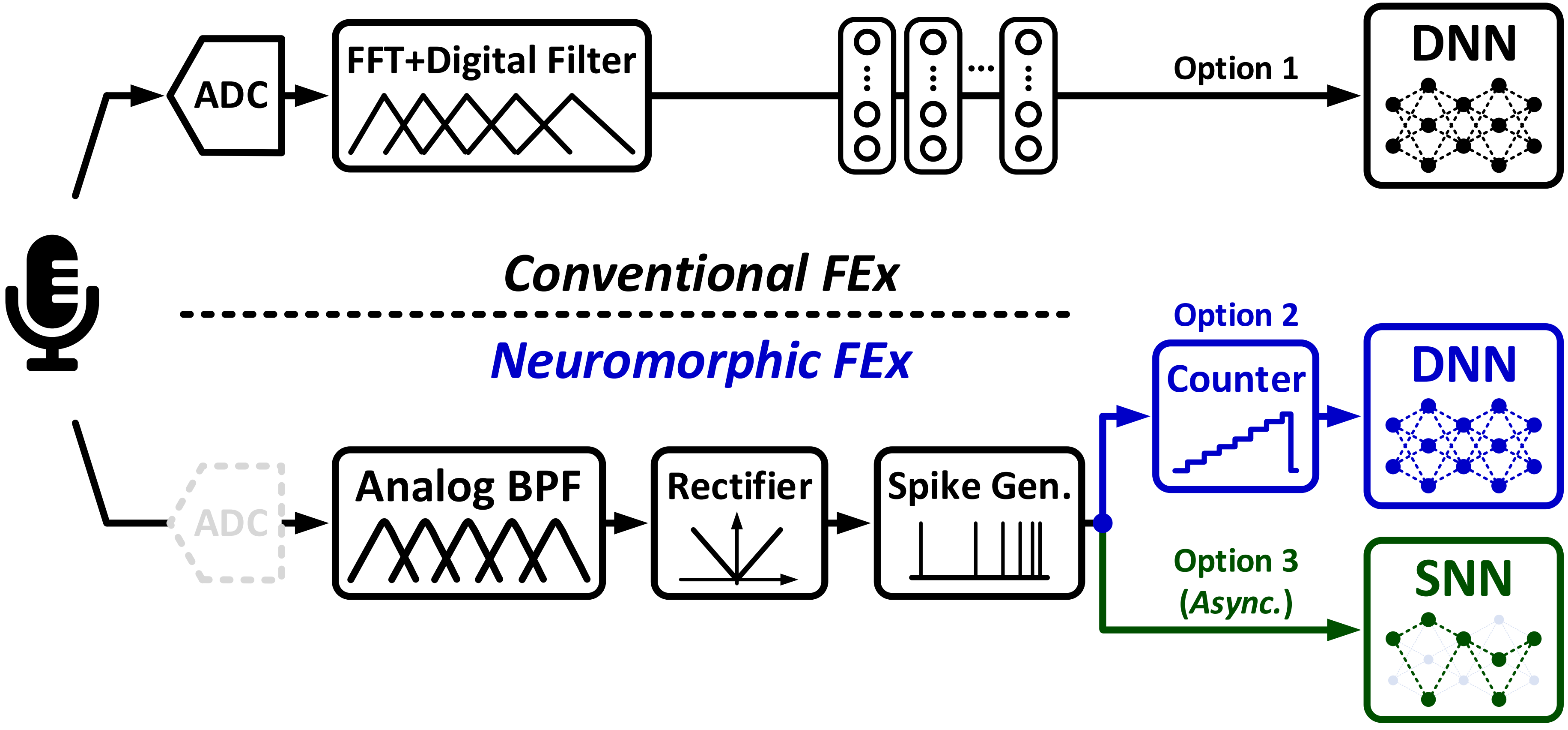




***Analog Signal Processing*** **is**

**More Efficient up to ~8-Bit Precision[1,2]**

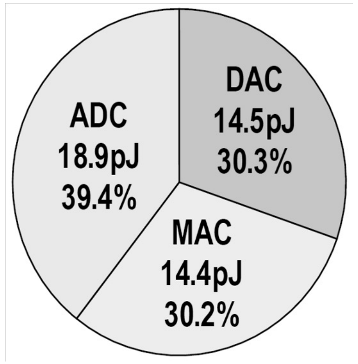
[1]R. Sarpeshkar, Neural Computation 1998 [2]B. Murmann, TVLSI 2021

# Why Neuromorphic Approach? – 3. Neural Network




**In-Memory Computing**

**$E_{ADC}+E_{DAC}$ ~ 58%[1]-70%[2] !**

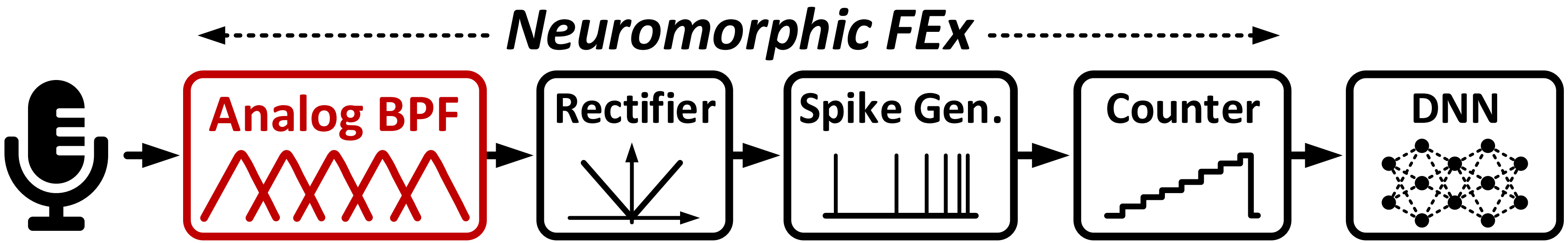


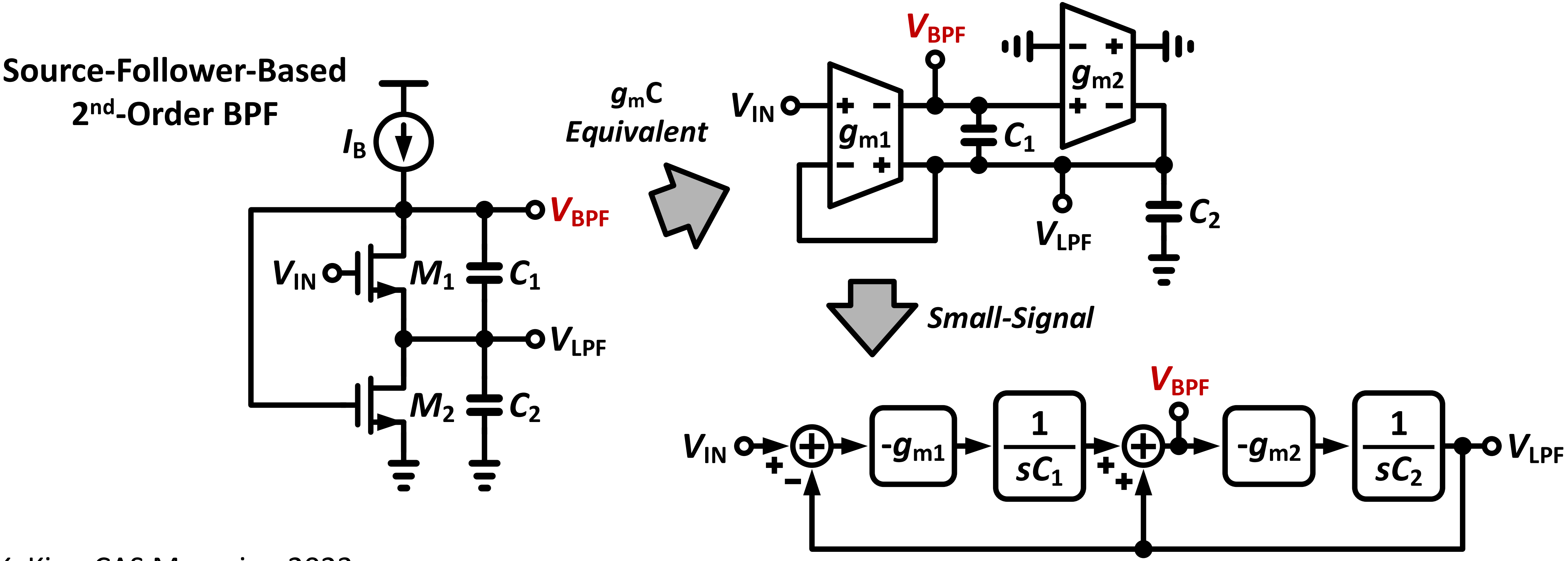

**Fully *Asynchronous***
**(or Fully Analog)**
**➔ No ADC & DAC**

**Spike-Based Interfaces can be**
**Seamlessly Integrated with *Asynchronous SNNs***

[1]A. Biswas, ISSCC 2018 [2]J.-O. Seo, ISSCC 2022

# Analog FEx (Voltage Domain)




K. Kim, CAS Magazine 2023

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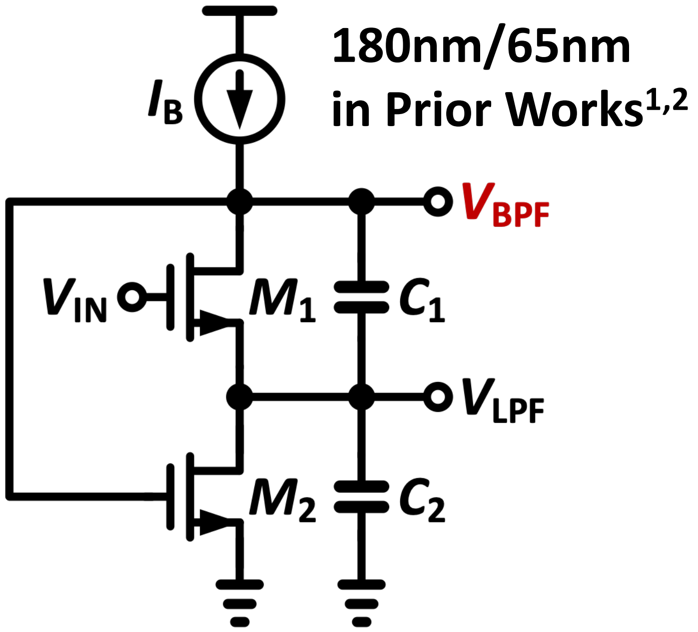
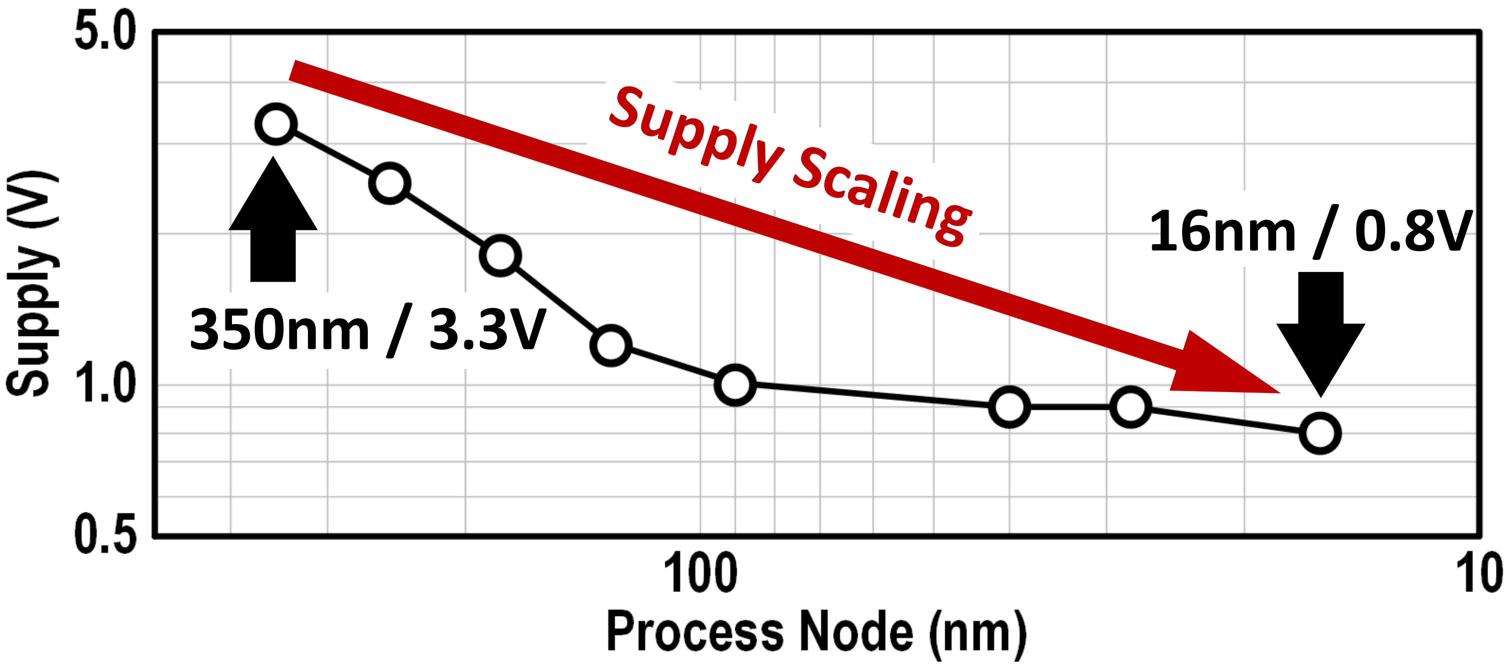



Source-Follower BPF

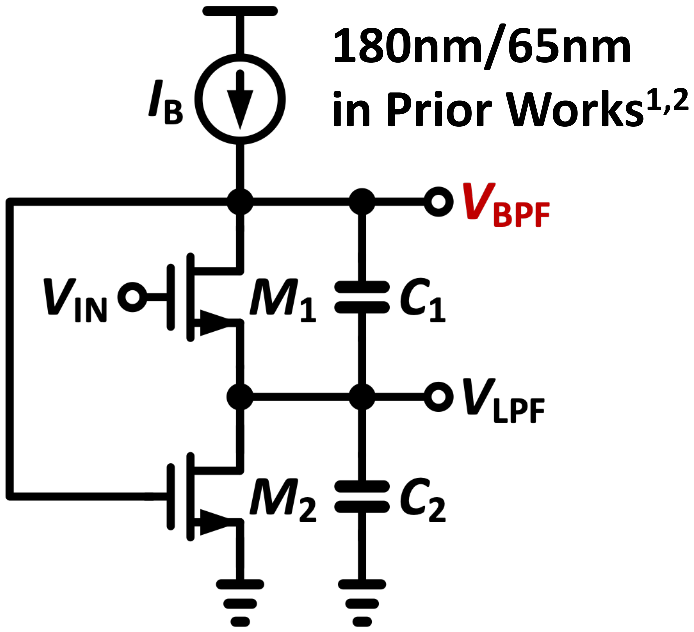



✘ Signal Swing (Headroom)
→ Reduced SNR

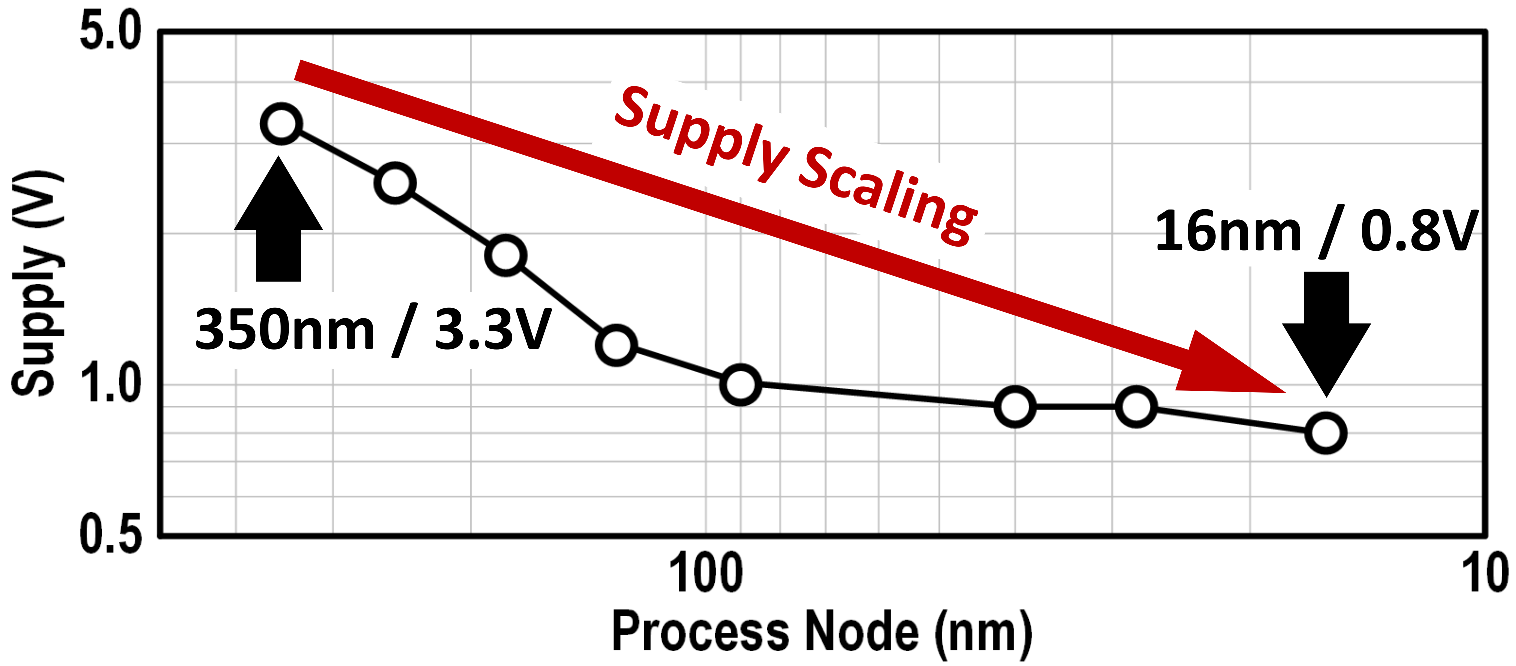
✘ DC Gain ($g_m r_O$)
→ Nonlinearity/Gain Error
→ Large L (Area/Power)

[1]M. Yang ISSCC 2018 [2]D. Wang, ISSCC 2021 [3]K. Kim, CAS Magazine 2023

# Analog FEx (Voltage Domain)



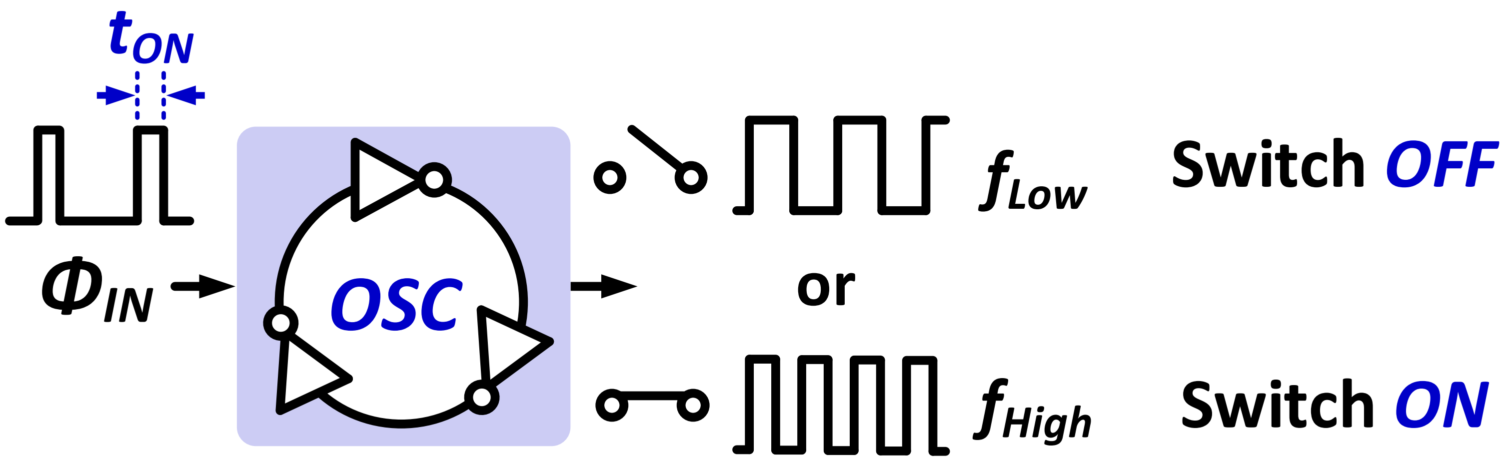
Source-Follower BPF




## Can Analog FEx Benefit from Technology Scaling?

[1]M. Yang ISSCC 2018 [2]D. Wang, ISSCC 2021 [3]K. Kim, CAS Magazine 2023

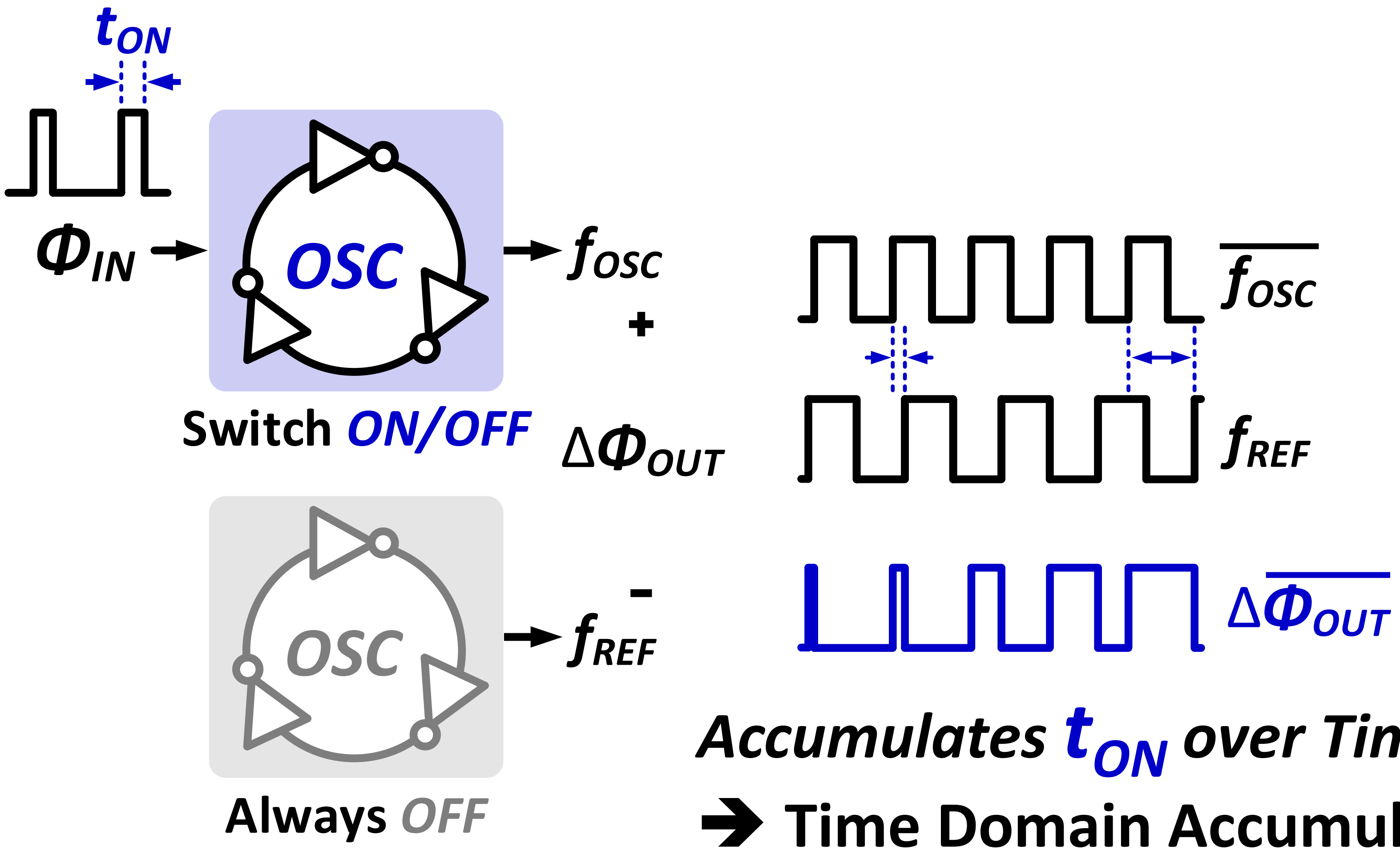
# Analog FEx (Time Domain)




**Average Frequency $\propto t_{ON}$**

B. Drost, ISSCC 2012 A. Elshazly, ISSCC 2012

# Analog FEx (Time Domain)



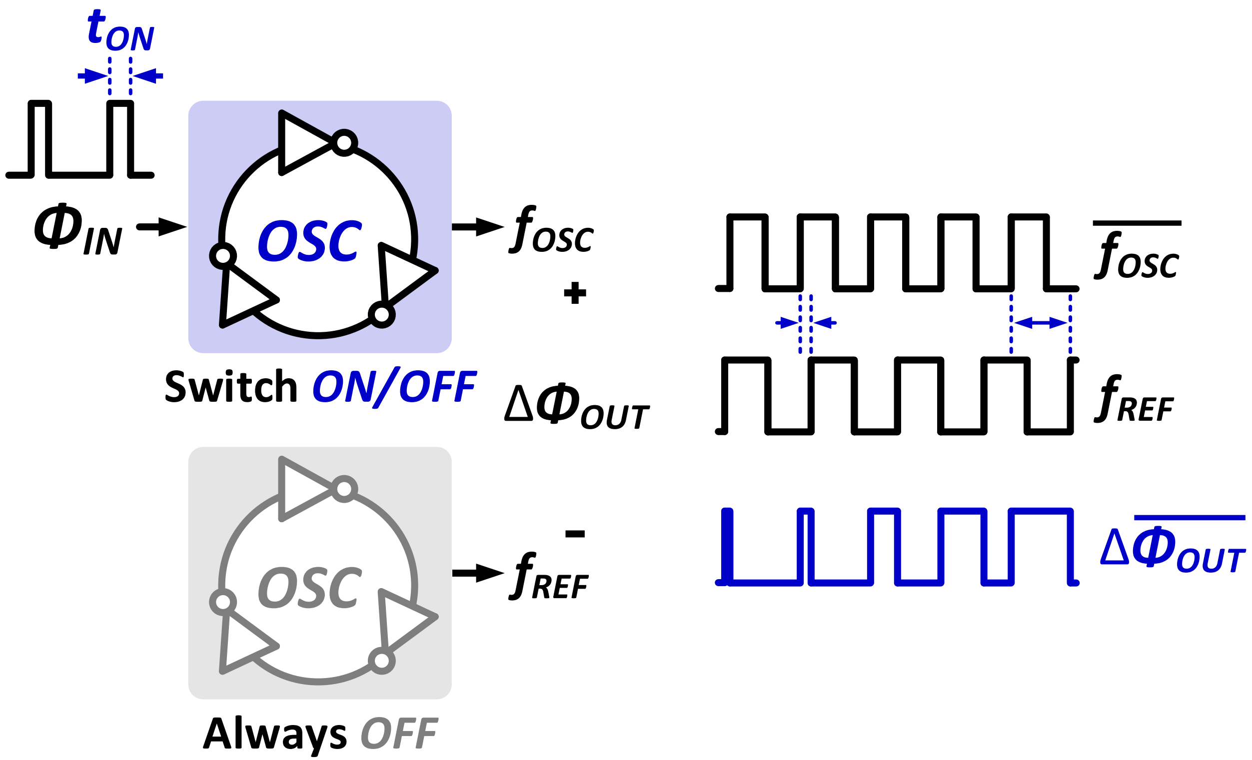

*Accumulates* $t_{ON}$ *over Time*

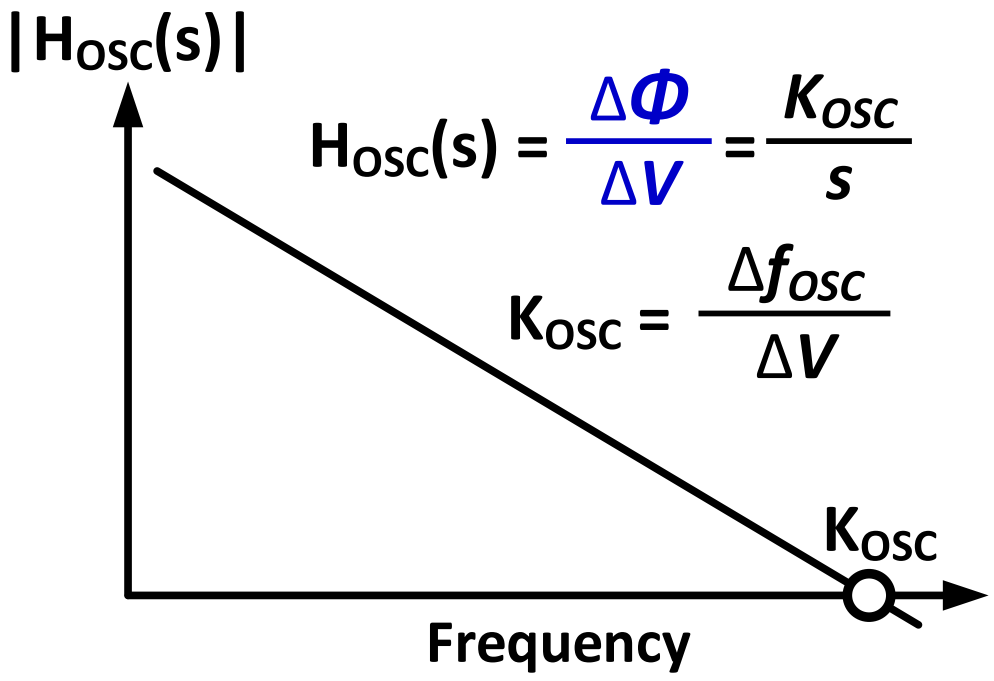
➔ **Time Domain Accumulator!**

B. Drost, ISSCC 2012

A. Elshazly, ISSCC 2012

# Analog FEx (Time Domain)



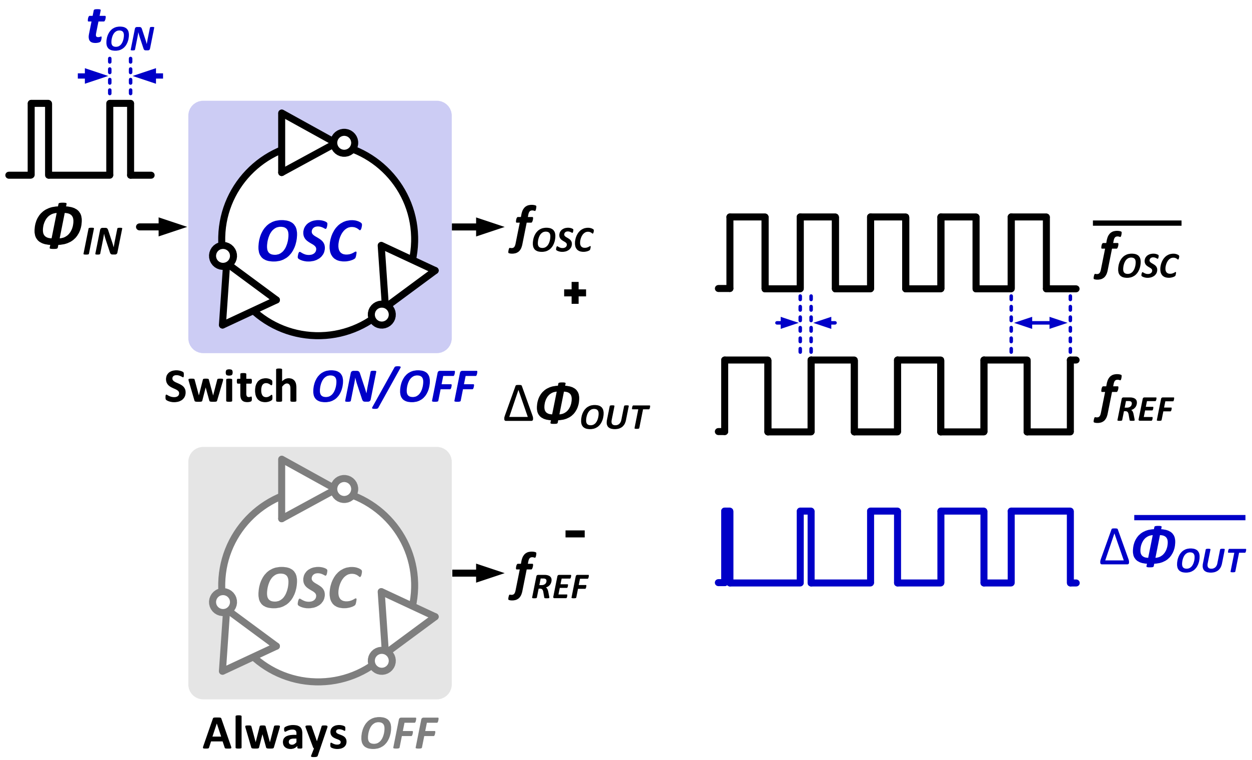

***Accumulates $t_{ON}$ over Time***

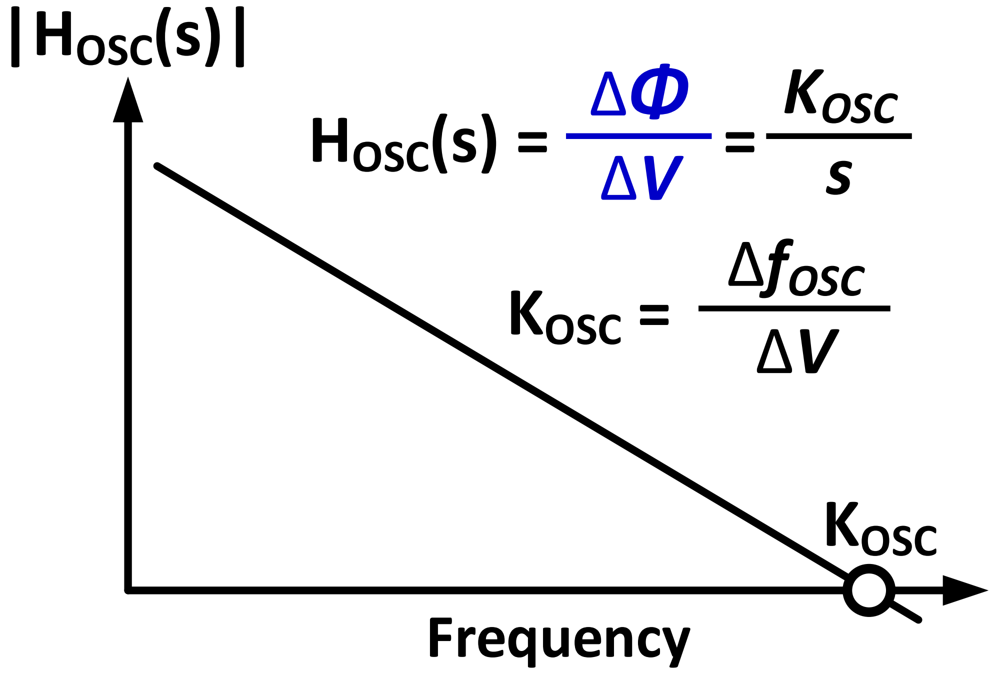
**➔ Time Domain Accumulator!**

**OSC is an Ideal Time-to-Phase Integrator**

B. Drost, ISSCC 2012 A. Elshazly, ISSCC 2012

# Analog FEx (Time Domain)



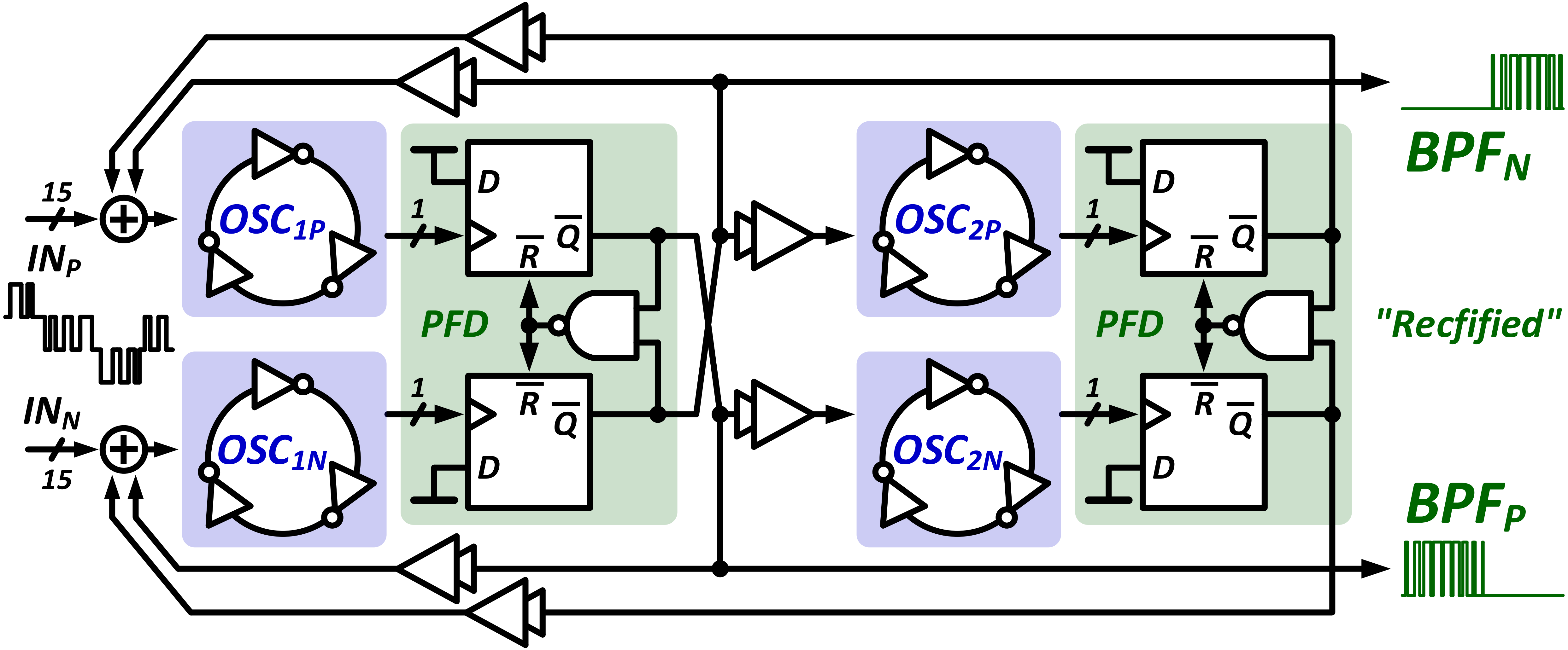

***Accumulates $t_{ON}$ over Time***

**➔ Time Domain Accumulator!**

- ✔ **Infinite** DC Gain
- ✔ **Free from** Signal Swing **Loss**
- ✔ Uses **Digital** Cells

B. Drost, ISSCC 2012 A. Elshazly, ISSCC 2012

# Time Domain 2nd-Order BPF w/ Inherent Rectification




K. Kim, ISSCC 2022 + JSSC 2022

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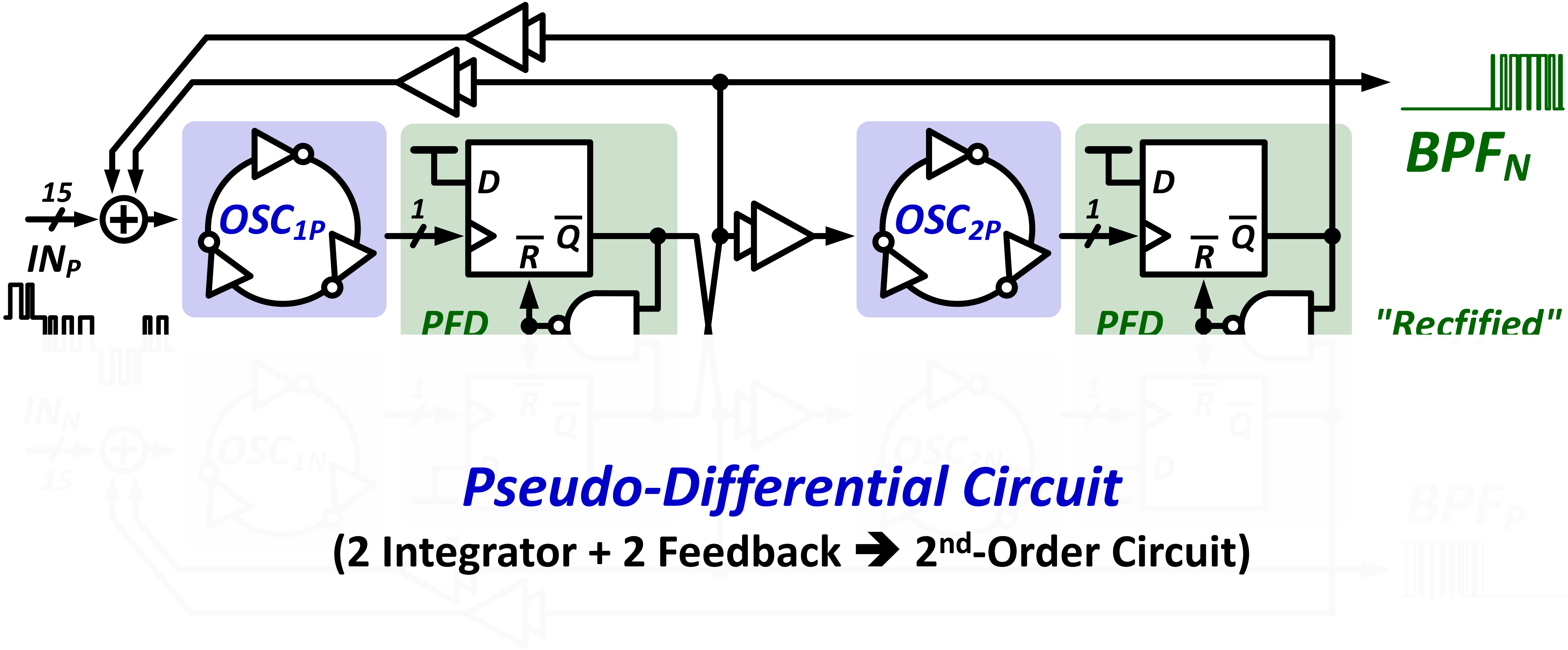


***Pseudo-Differential Circuit***

**(2 Integrator + 2 Feedback ➔ 2nd-Order Circuit)**

K. Kim, ISSCC 2022 + JSSC 2022

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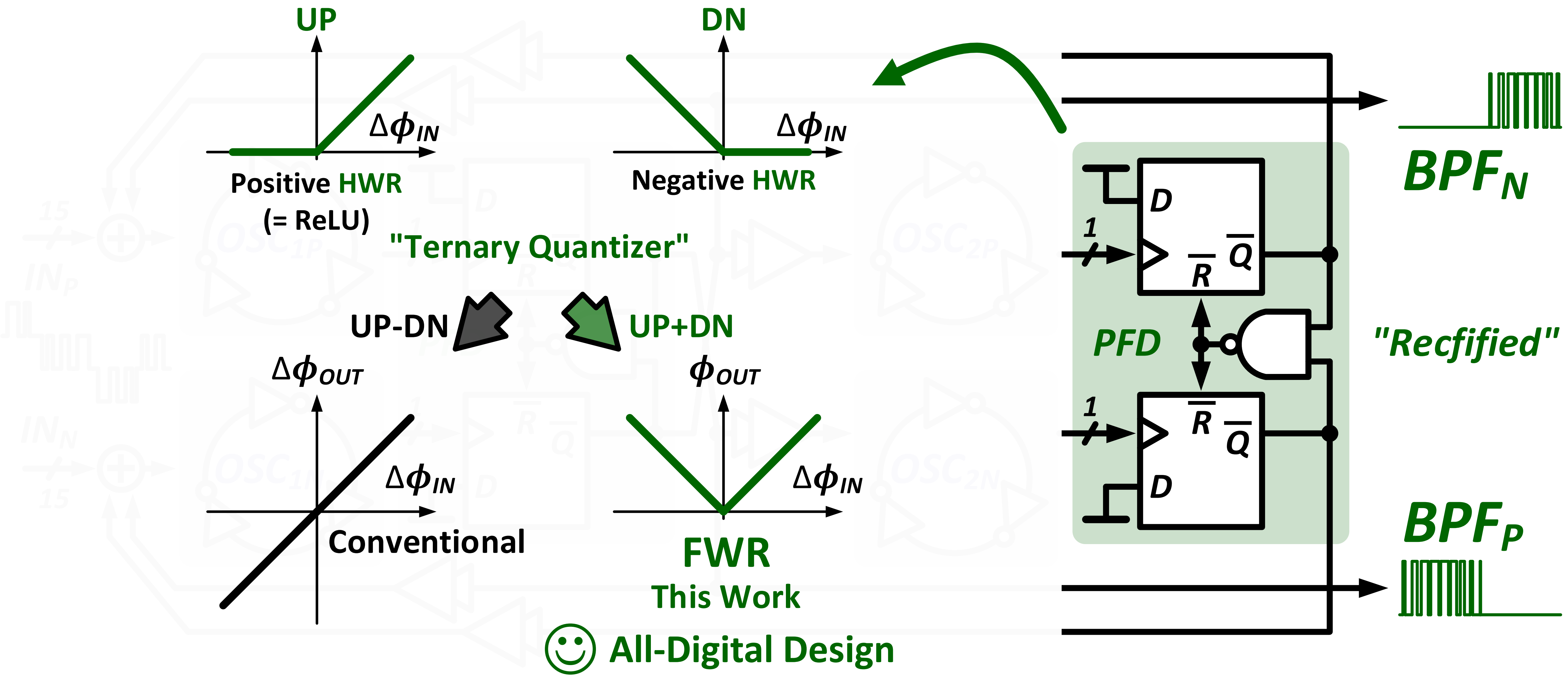
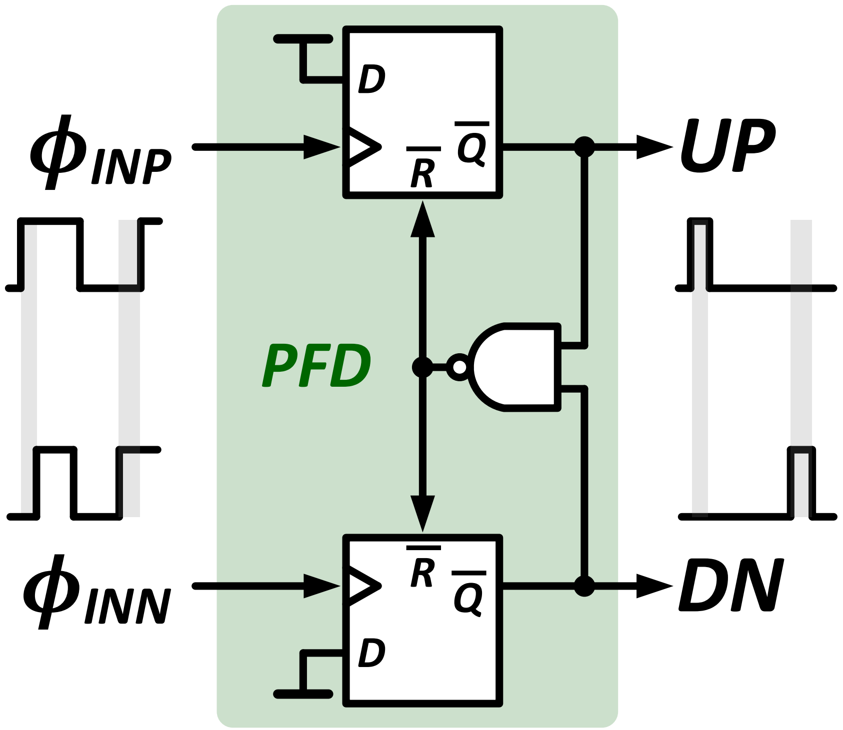



K. Kim, ISSCC 2022 + JSSC 2022

*HWR/FWR: Half/Full-Wave Rectifier

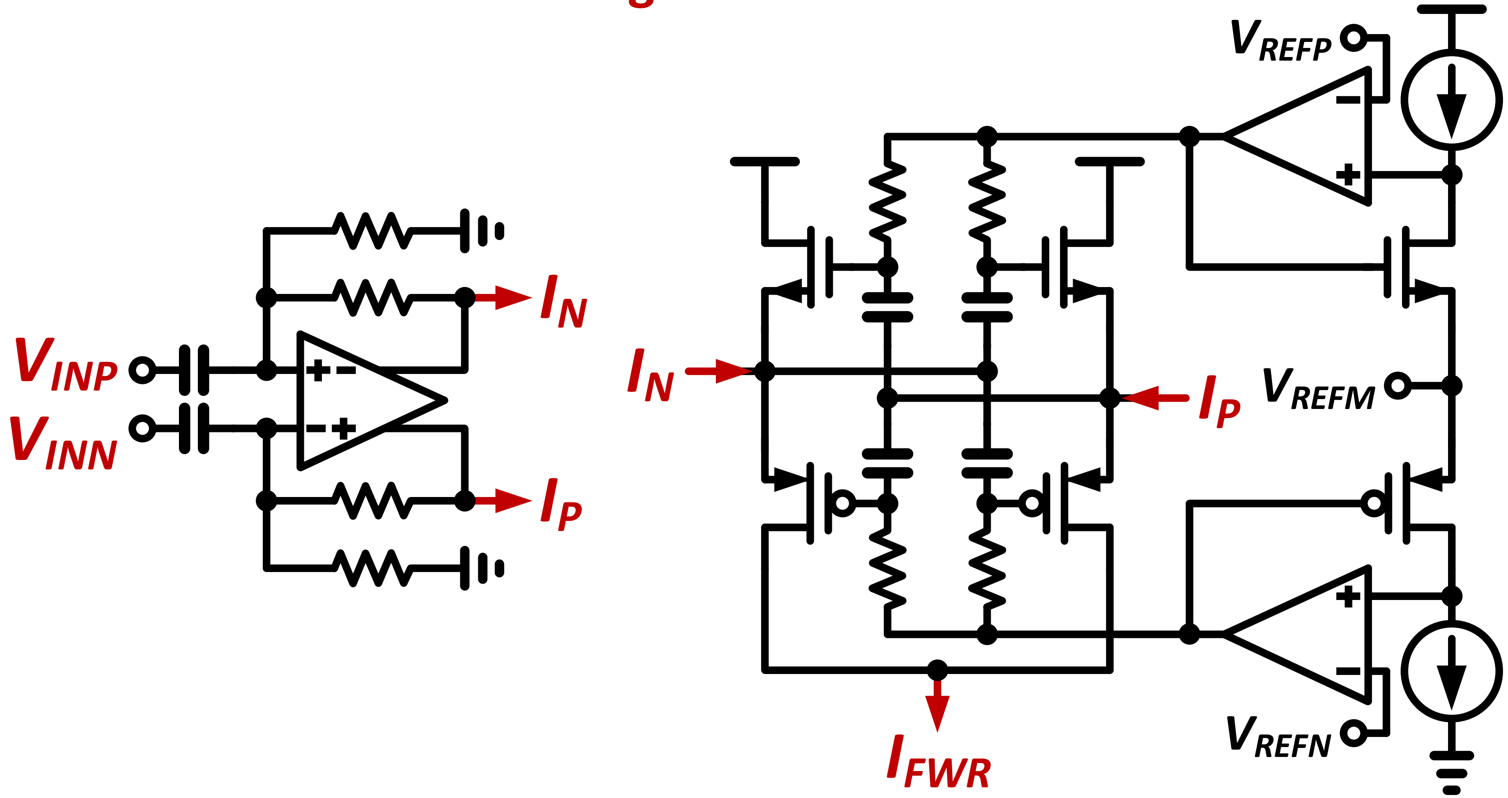
# Time Domain[1] vs Voltage Domain[2] Rectifiers

## Time-Domain FWR




2 D-FF + 1 NAND

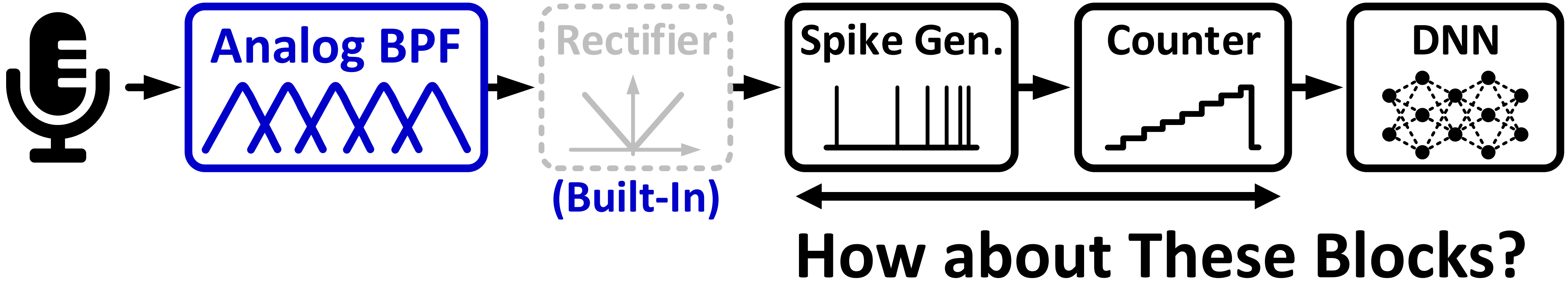
## Voltage-Domain FWR



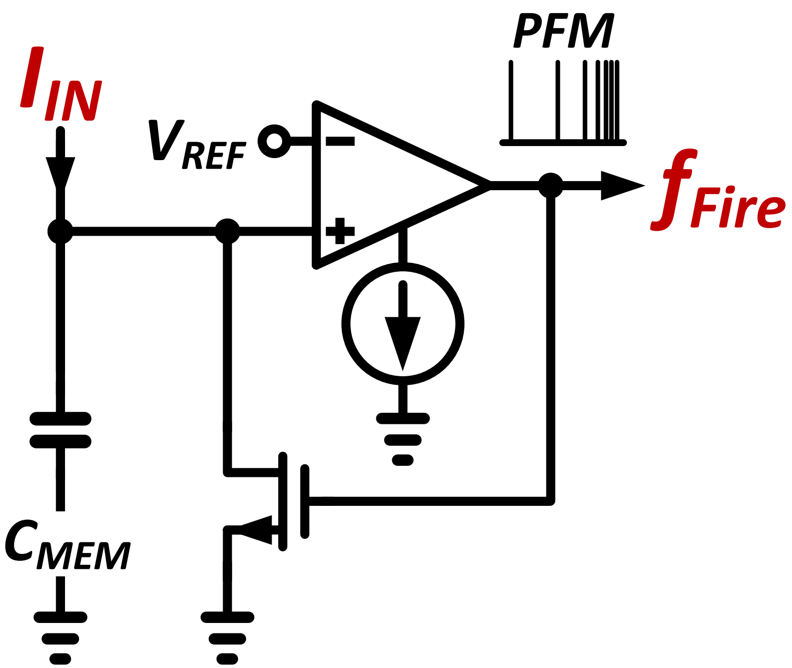

3 OTAs + 2 $I_{BIAS}$ + 3 $V_{REF}$ + 8 Resistors + 6 Capacitors

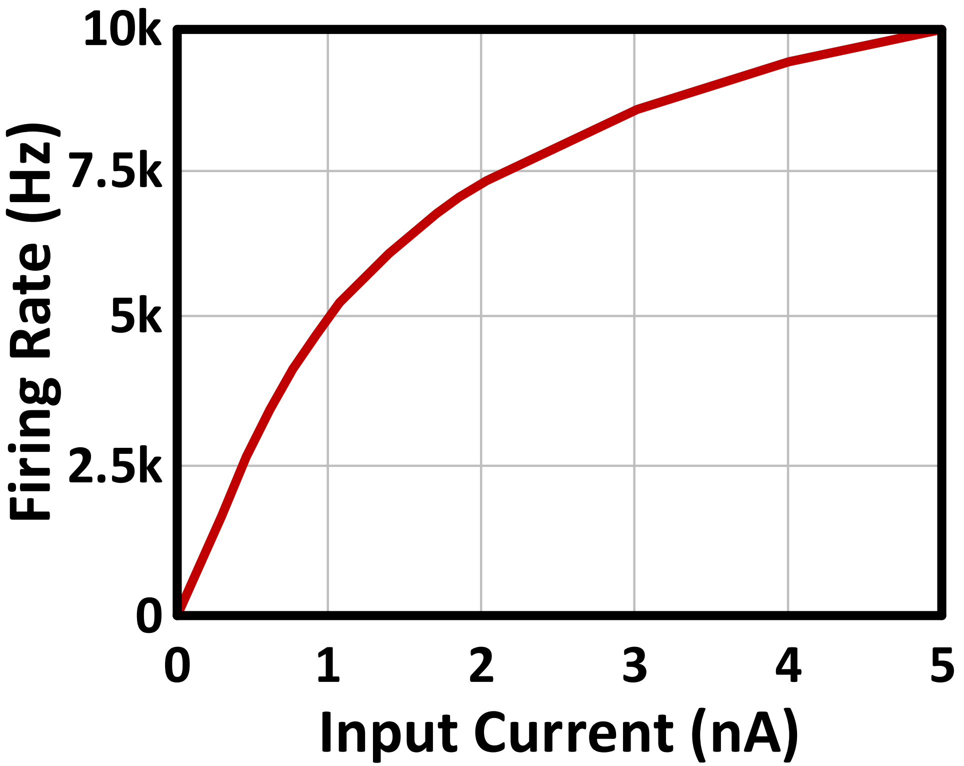
[1]K. Kim, ISSCC 2022 [2]M. Yang, ISSCC 2018

# Time Domain Neuromorphic FEx



# Integrate-Fire (IF) Neuron (Voltage Domain)

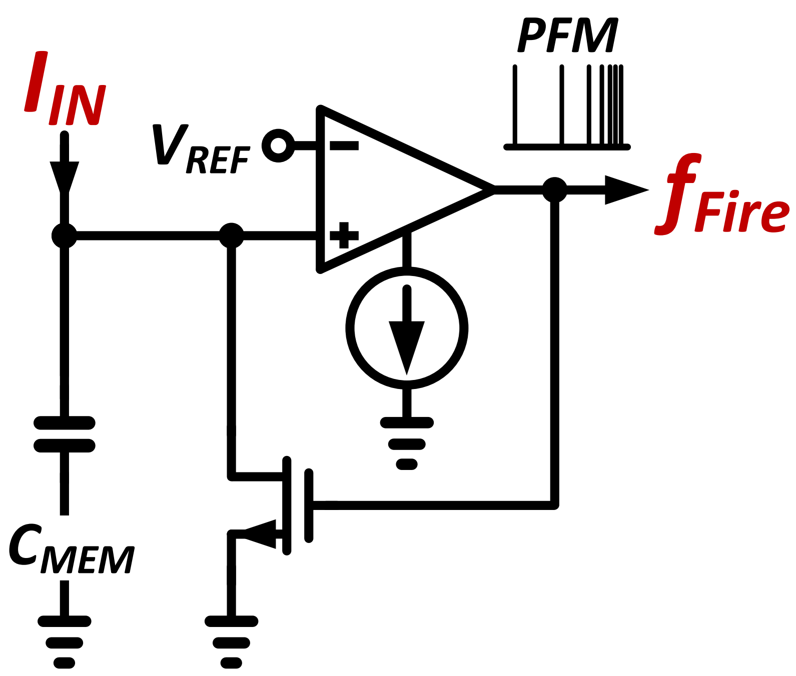


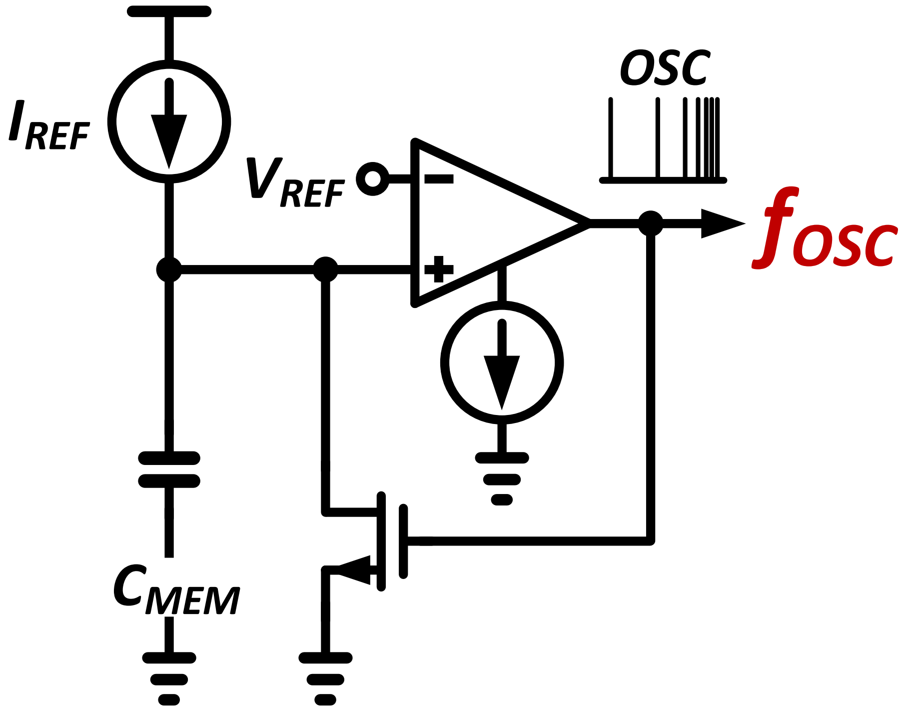

**IF Neuron[1] Has Been Widely Adopted in Building Blocks of Analog Neuromorphic Circuits**

[1]C. Mead, 1989

# Integrate-Fire (IF) Neuron (Voltage Domain)




IAF Neuron[1]

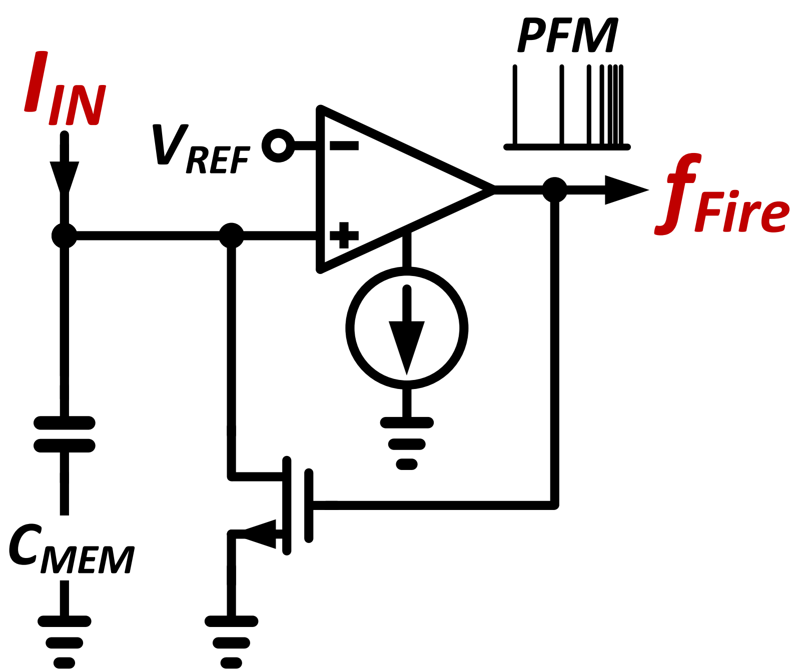


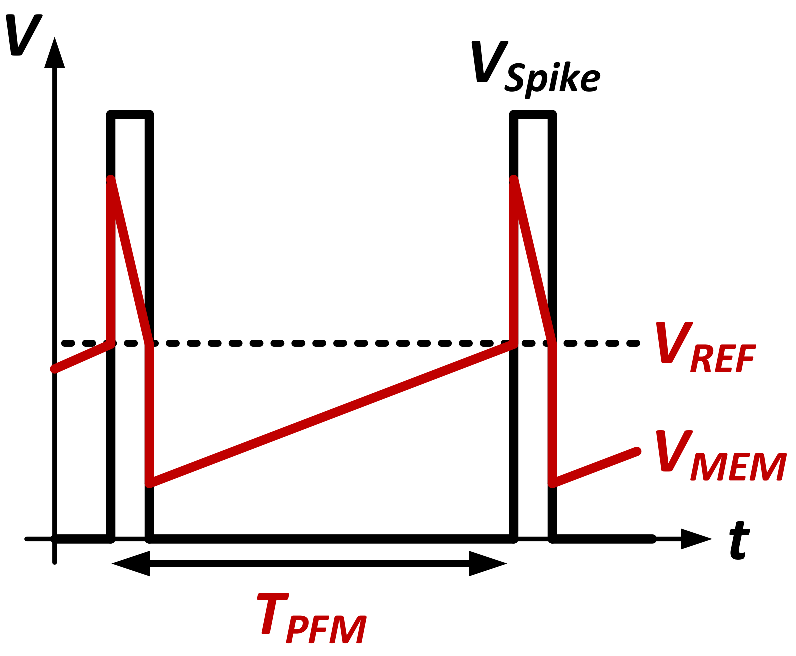

Relaxation Oscillator[2]

**IF Neuron[1] Can be Interpreted as**
**a Current-Controlled Relaxation Oscillator[2]**

[1]C. Mead, 1989 [2]A. A. Abidi, JSSC 1983

# Integrate-Fire (IF) Neuron (Voltage Domain)



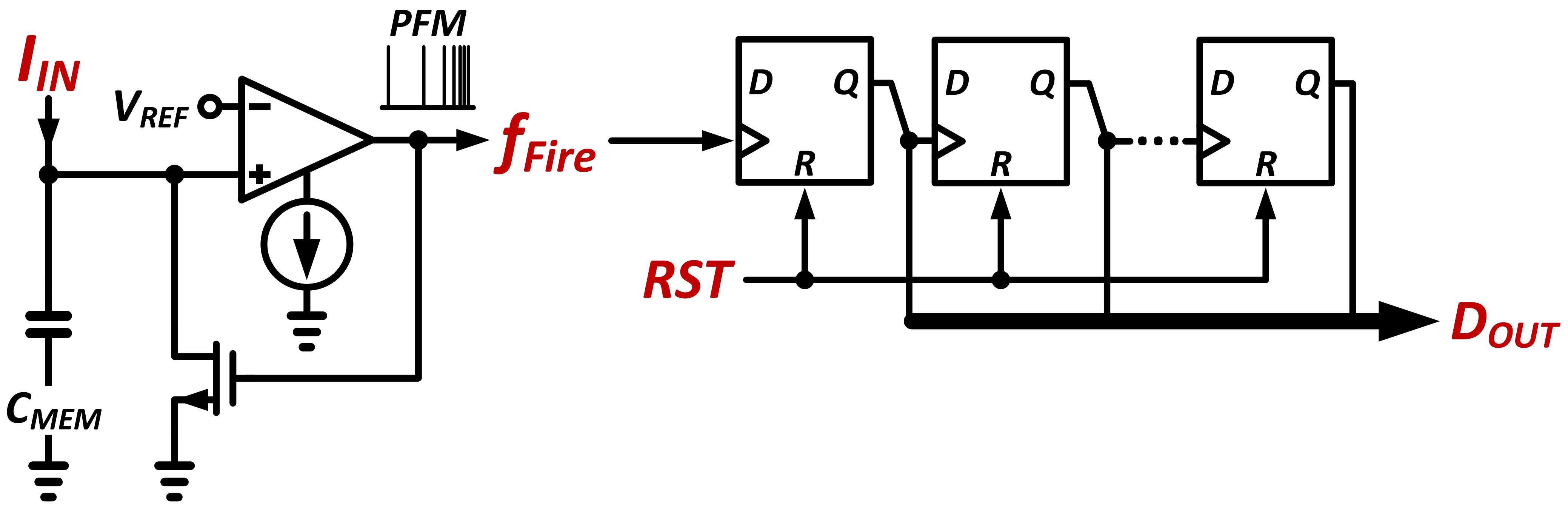

**Regarding Technology Scaling?**

**Voltage Domain Integral ($V_{MEM}$)**

**✘ Headroom** **✘ Static Comparator**

C. Mead, 1989

# Integrate-Fire (IF) Neuron (Voltage Domain)



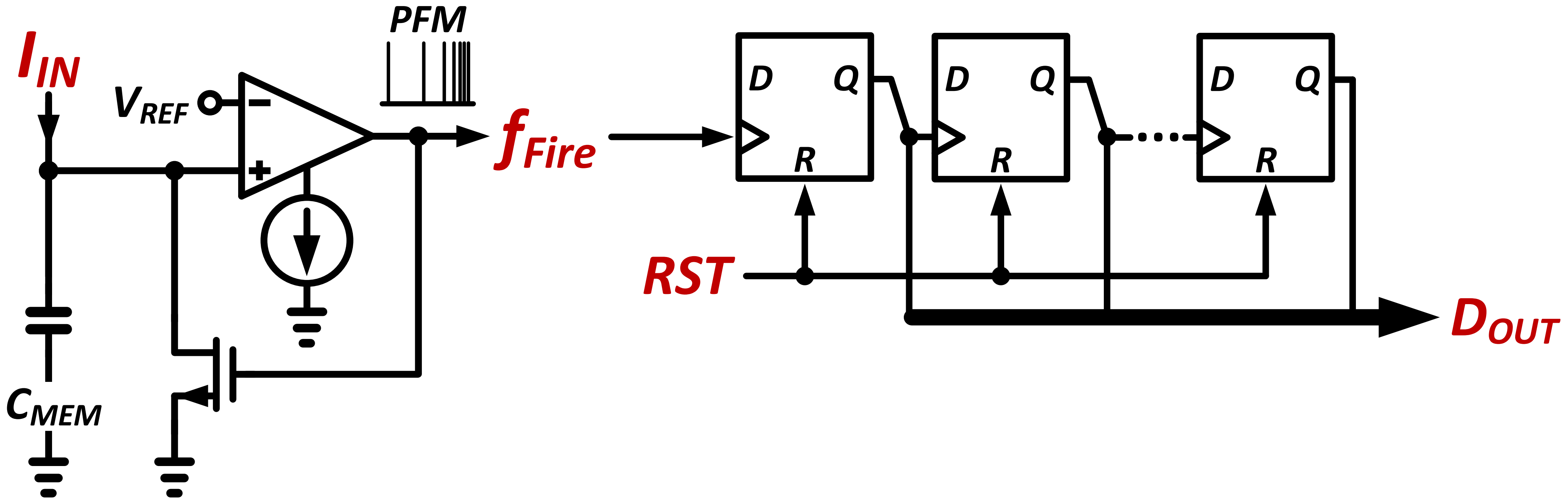

**With Spike Counter?**

**Current-Controlled Oscillator (CCO)**

**Ripple Counter (Frequency Quantizer)**

M. Yang, ISSCC 2018 D. Wang, ISSCC 2021

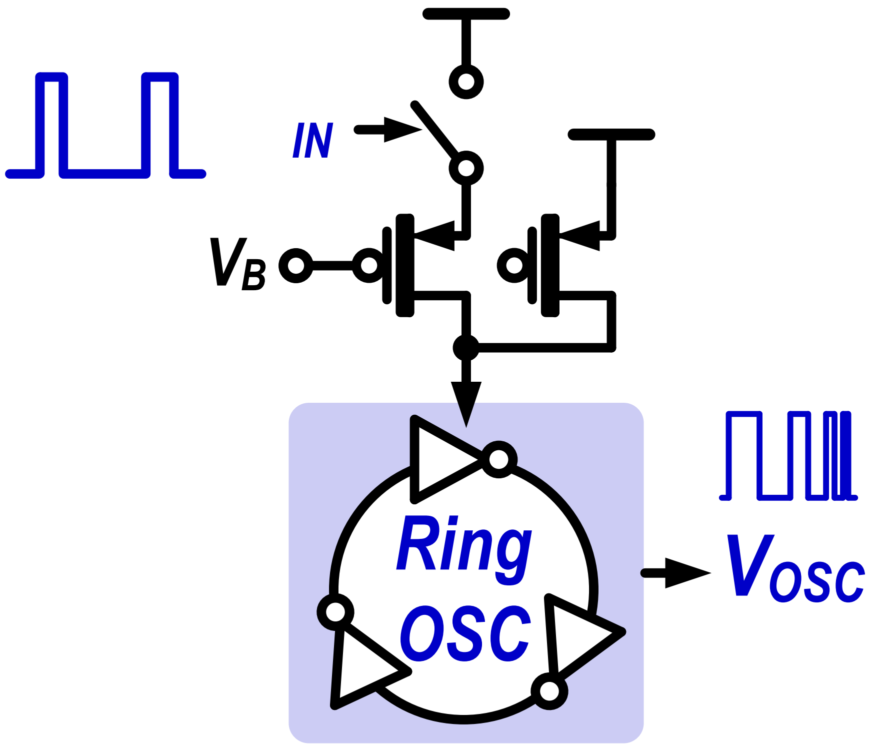
# Integrate-Fire (IF) Neuron (Voltage Domain)

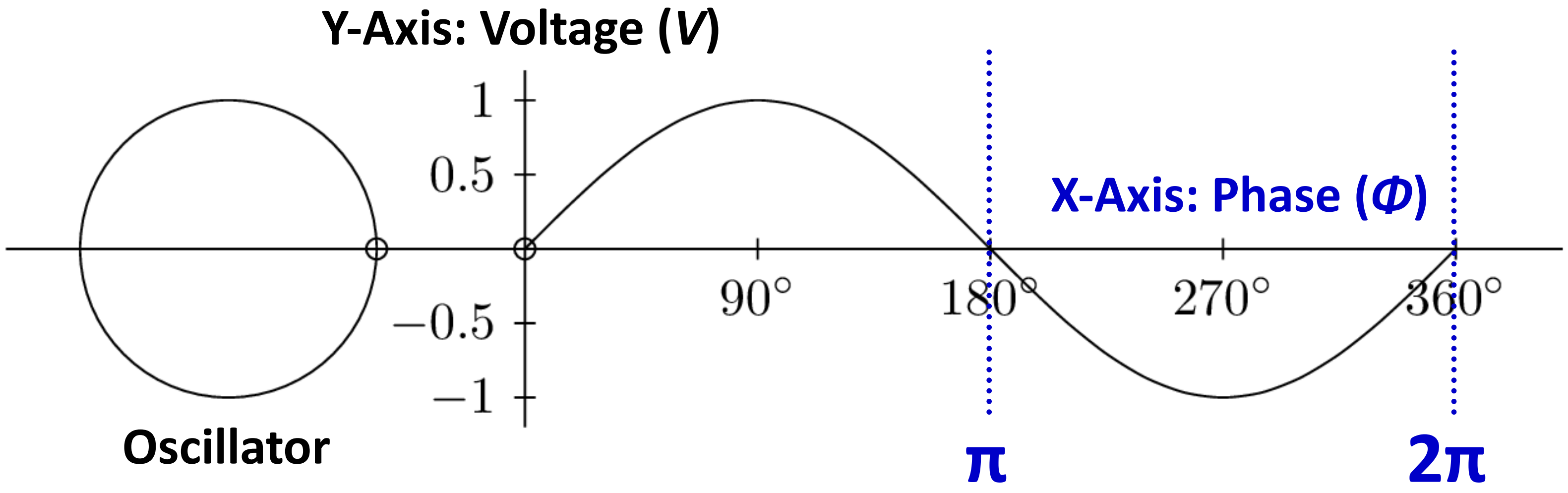



➔ **CCO-Based ΔΣ Modulator !**

M. Straayer, JSSC 2008 J. Kim, TCAS-I 2010

# Integrate-Fire (IF) Neuron (Time/Phase Domain)

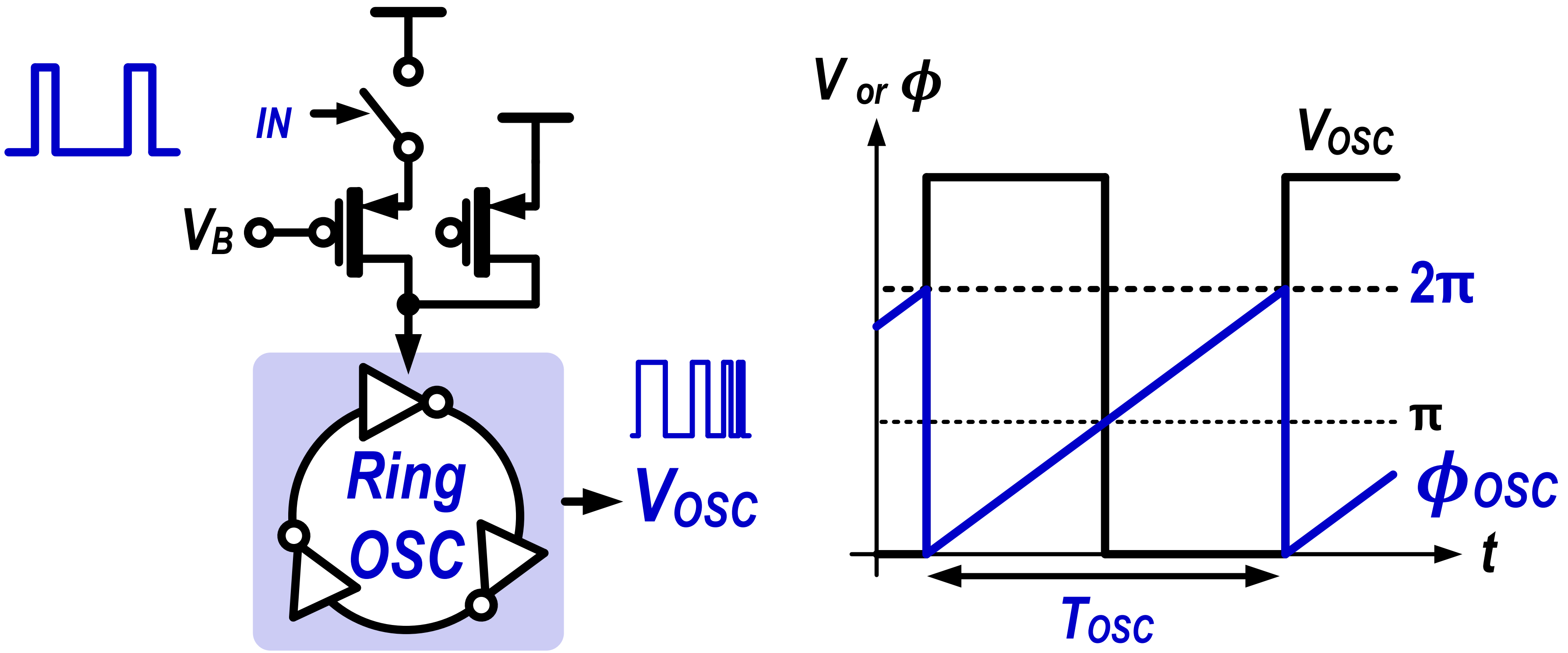



**Phase Domain IAF Neuron ($\Phi_{OSC}$)**

K. Kim, ISSCC 2022 + JSSC 2022

# Integrate-Fire (IF) Neuron (Time/Phase Domain)



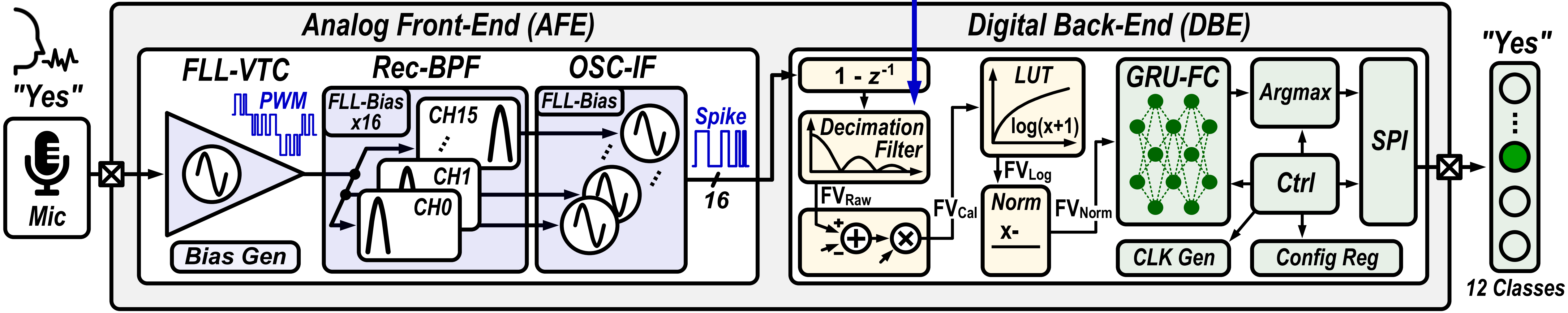

**Phase Domain IAF Neuron ($\Phi_{OSC}$)**

- ✔ Technology Scalable
- ✔ No Static Comparator (Inherent 2π Threshold)

K. Kim, ISSCC 2022 + JSSC 2022

# Neuromorphic Keyword Spotting Chip

To Filter Out ΔΣ Q-Noise




Ring-Oscillator-Based
**Time Domain** Feature Extractor
(Technology Scalable)

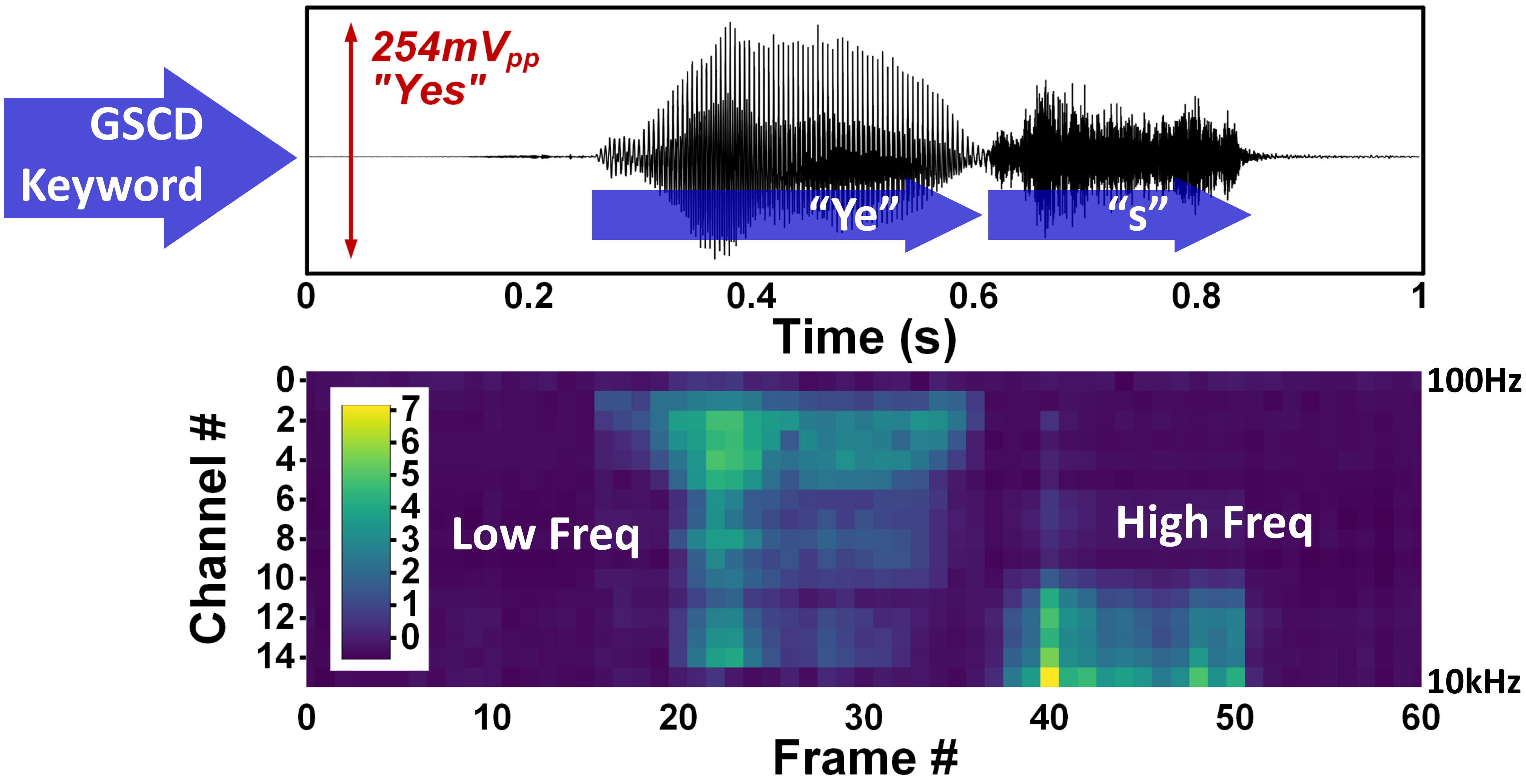
GRU-FC RNN Classifier

***The First Chip*** **and** ***The Only Chip*** **that integrates**
**Time Domain Analog FEx + Digital Classifier all on-chip, even to date**

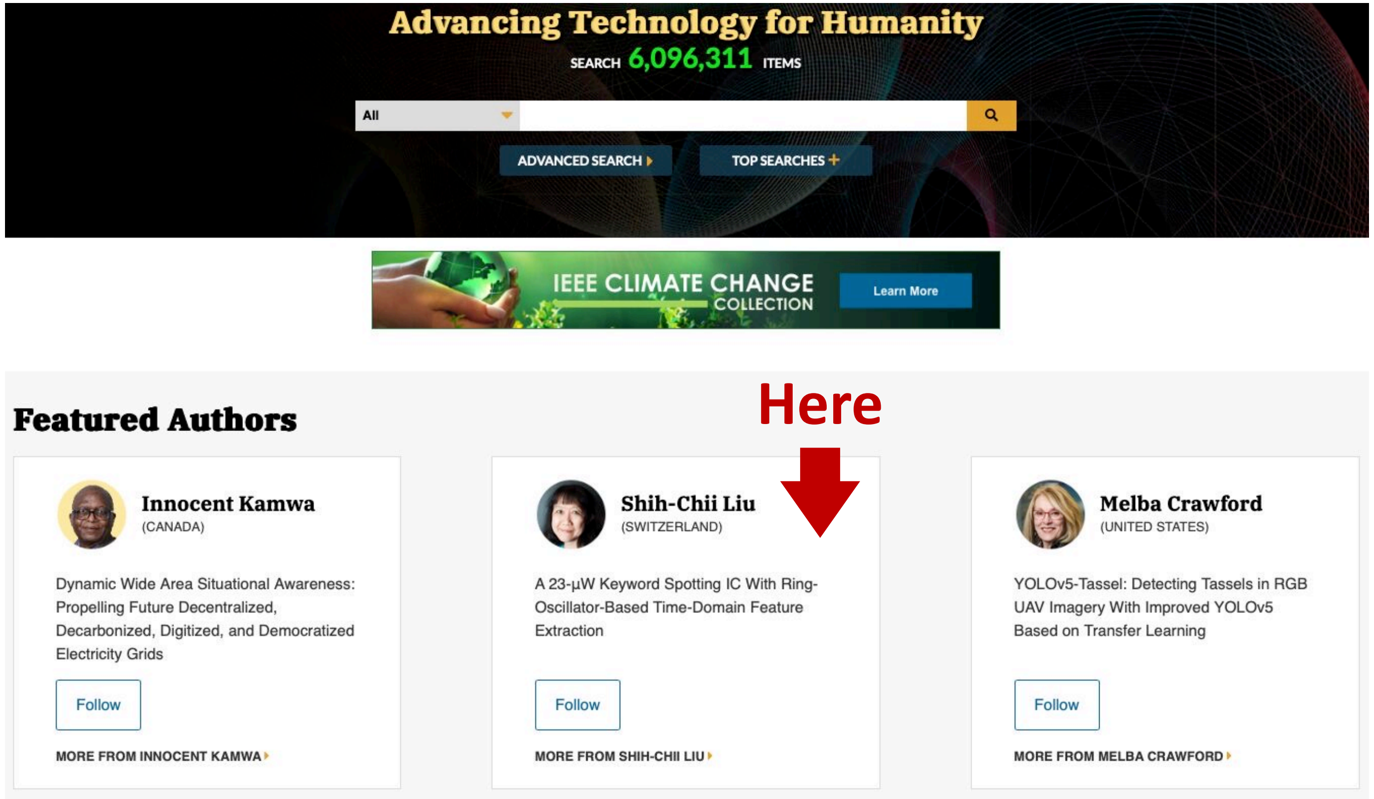
K. Kim, ISSCC 2022 + JSSC 2022

# Audio Response of FEx

**GSCD:** Google Speech Command Dataset



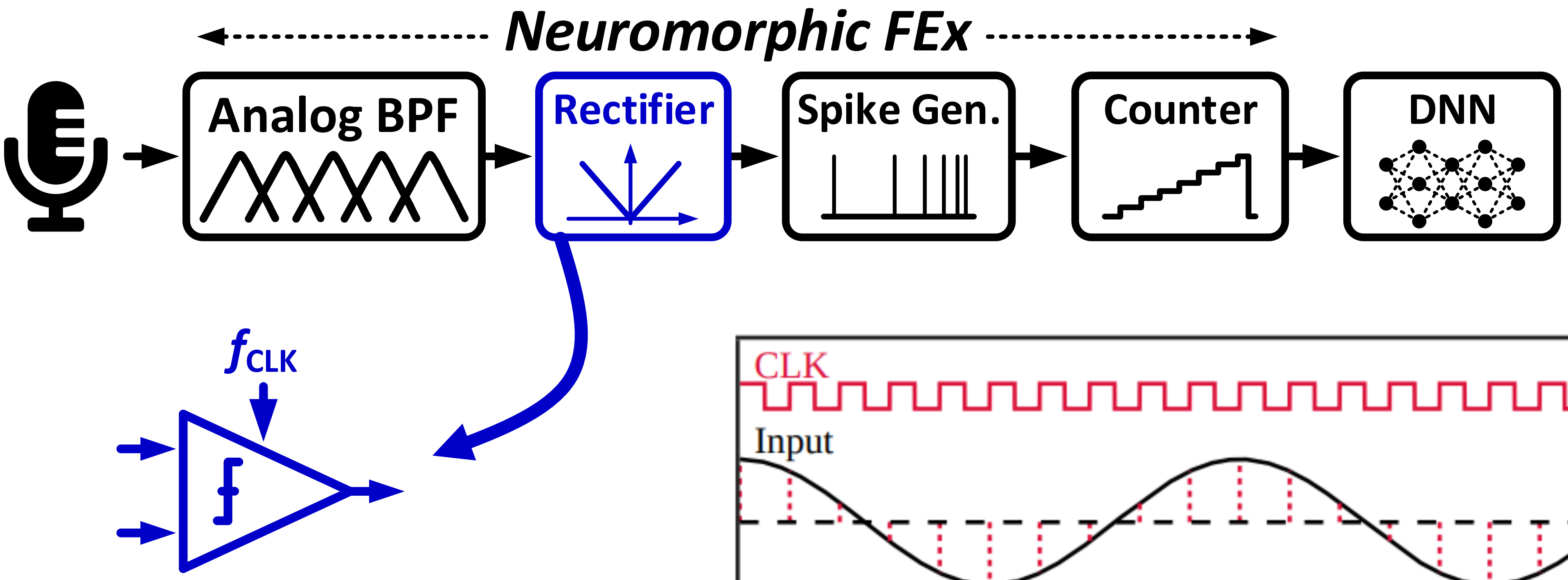
# IEEE Highlights (Sep. ~ Oct. 2023)



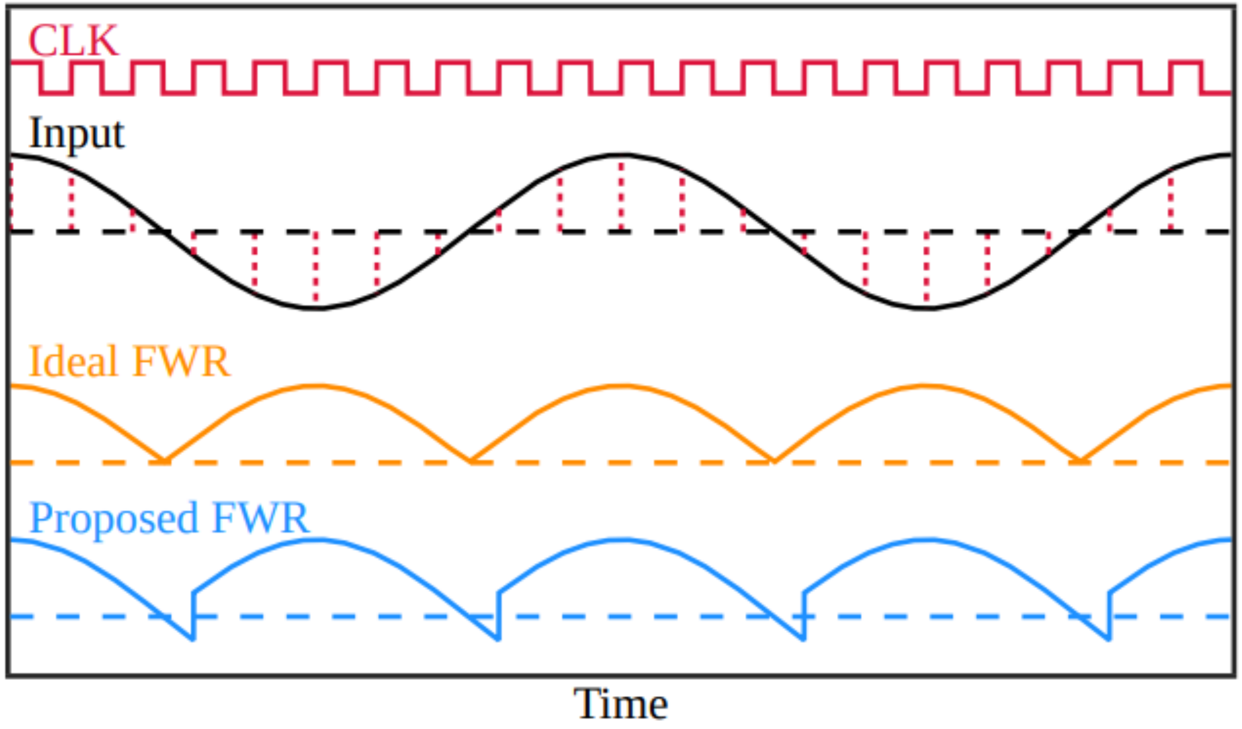

(IEEEXplore Main Page)


**Please Find Design Secrets in JSSC 2022 Paper!**

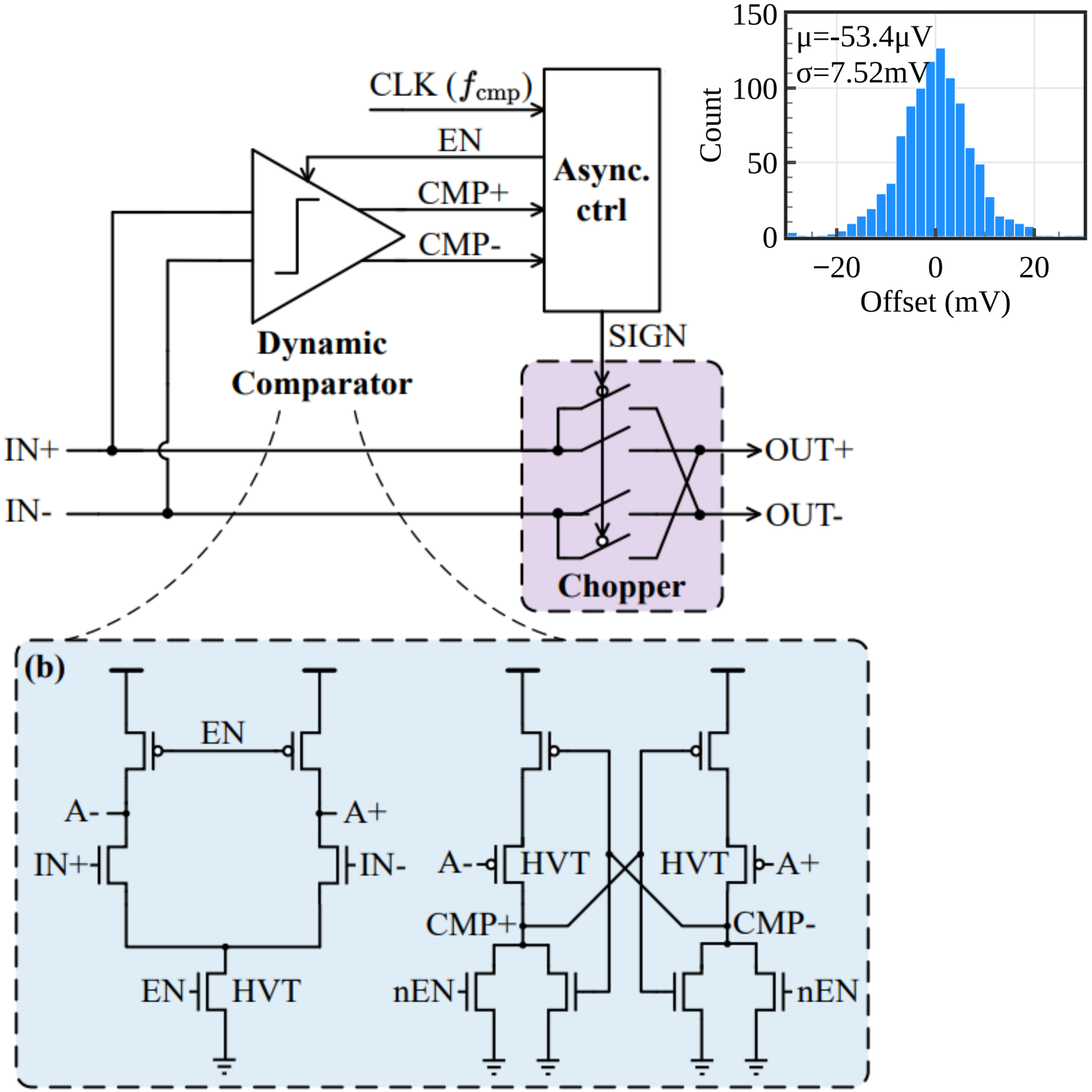
# Hardware-Aware Algorithm Optimization



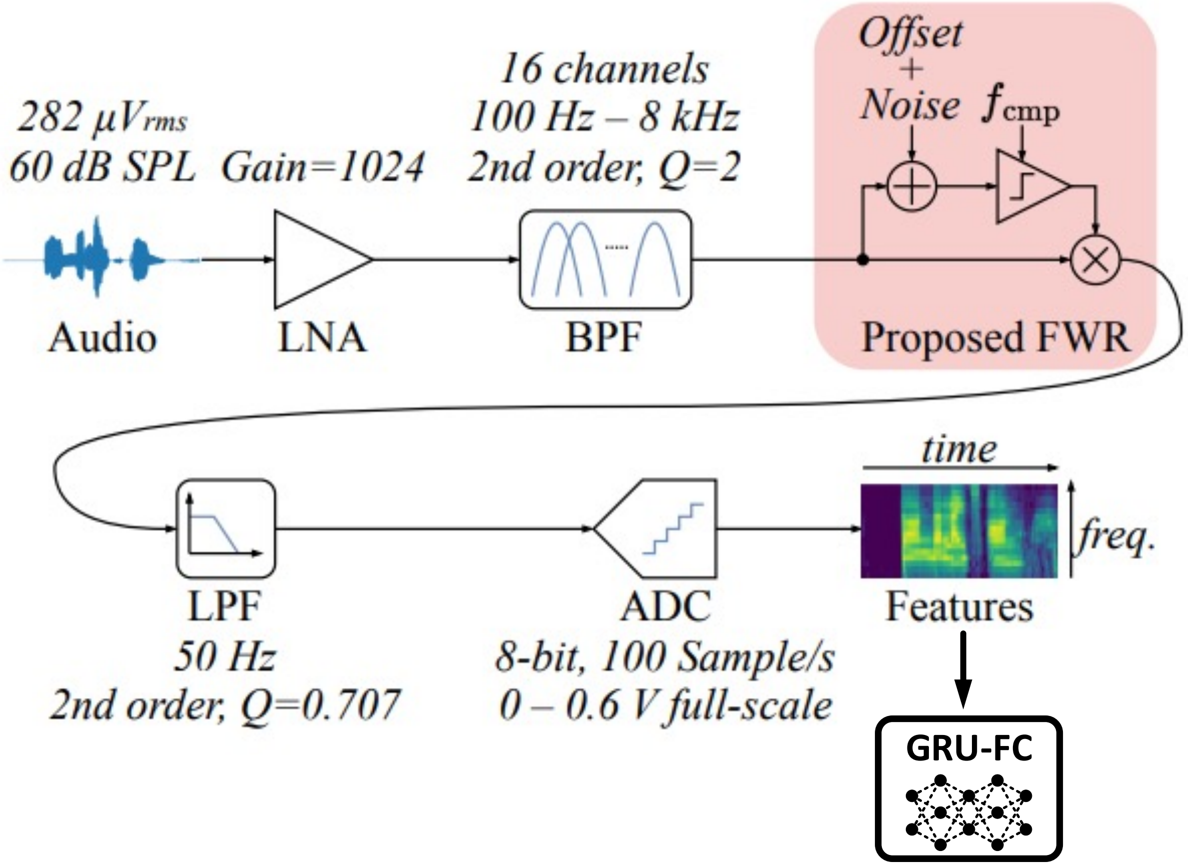

**What If We Use**
**a Dynamic Comparator**
**To Rectify The Signal?**



# Hardware-Algorithm Co-Optimization




**Analog Circuits are Python-Modeled, Included into RNN Training Loop Under PyTorch Framework**




S. Zhou, AICAS 2023

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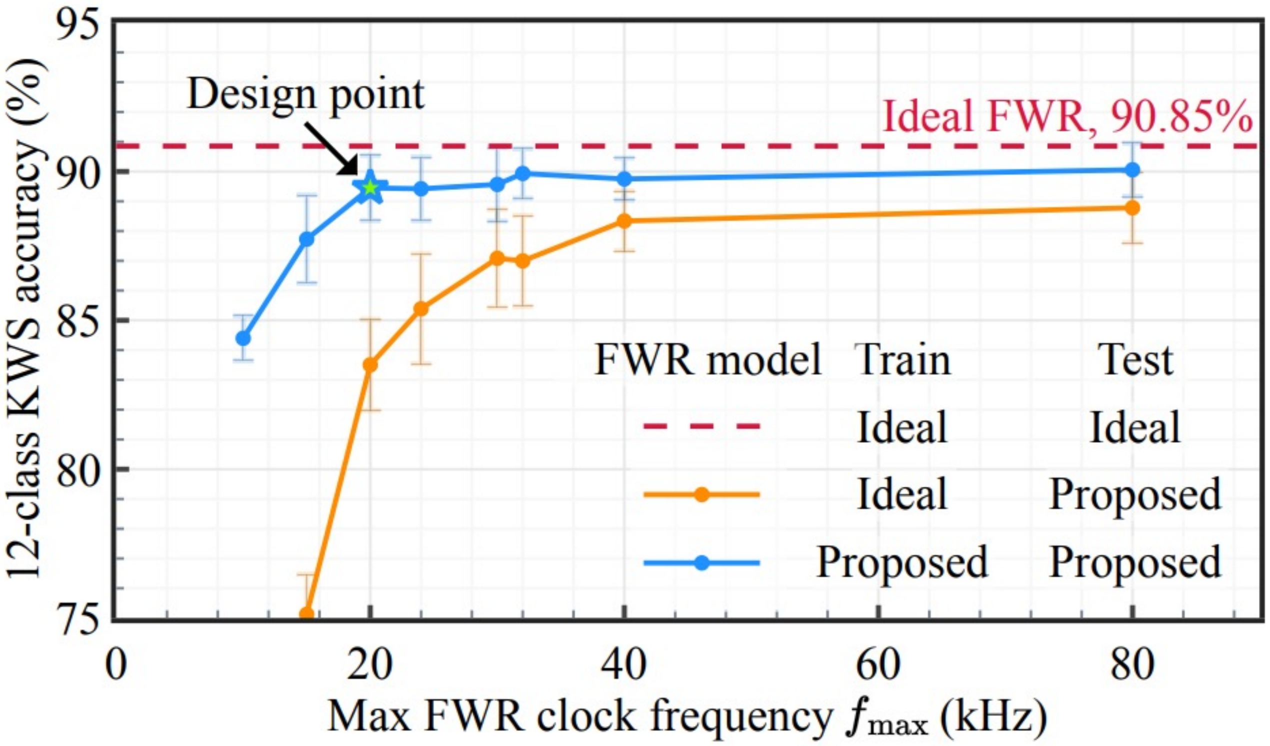



**Hardware-Aware Training**

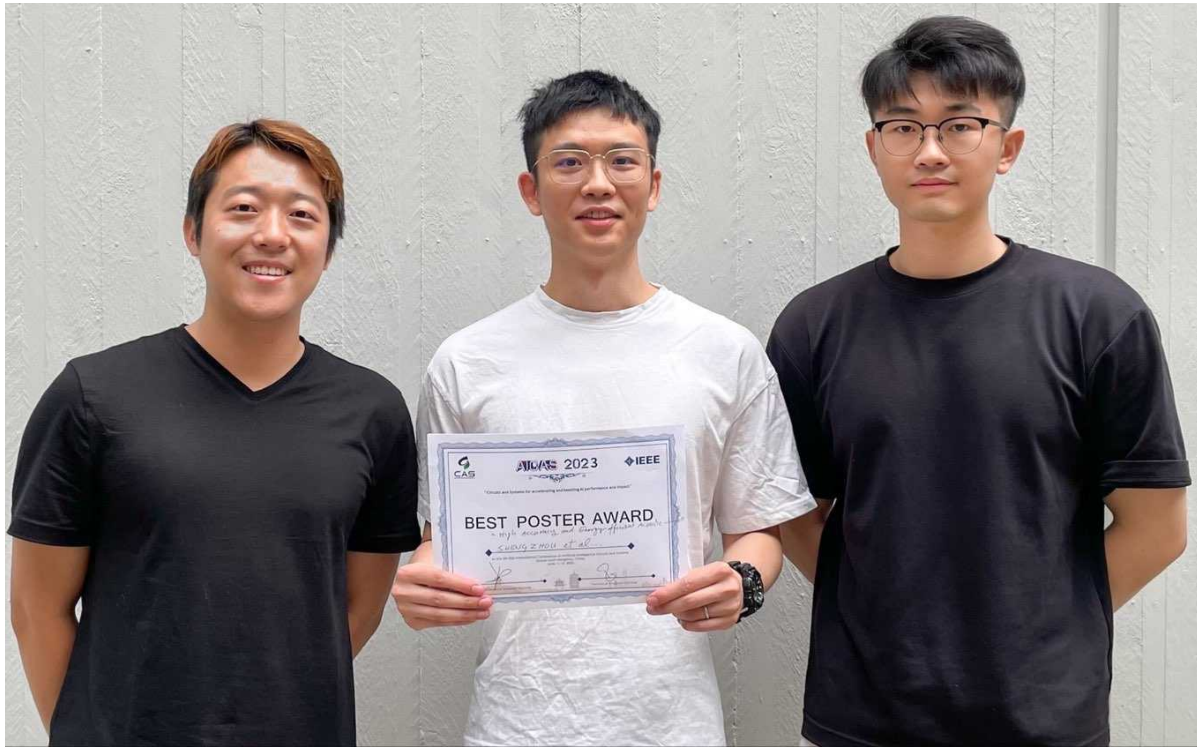
- ✓ **Negligible** Accuracy Loss
- ✓ **31.2x** Less Rectifier Power than State-of-the-Art
- ✓ **Without** Increase of Network Size

S. Zhou, AICAS 2023

# AICAS 2023 Best Poster Award

## High-Accuracy and Energy-Efficient Acoustic Inference using Hardware-Aware Training and a 0.34 nW/Ch Full-Wave Rectifier

Sheng Zhou*, Xi Chen*, Kwantae Kim, Shih-Chii Liu
Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland
{shengzhou, xichennn, kwantae, shih}@ini.uzh.ch



# Outline

- Visions of IoT Sensors
- Biomedical Sensor
- Neuromorphic Sensor
- **Outlook**

# Summary

- **Tiny, Sensory, Intelligent, Wireless IoT Platforms**
- **Bioimpedance Sensor**
- **Neuromorphic Sensor**
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  - Will Enrich Our Daily Lives in the Next 10 Years
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  - Open-Sourced Circuit Designs!
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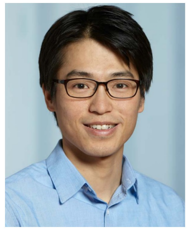
  - New Opportunities with Hardware-Aware Algorithms
- **Outlook**
  - Multiple Cross-Domain / Interdisciplinary Research Opportunities
  - Wireless TRx, Device-Circuit, Circuit Theory, Vocal Studies, …

# Acknowledgments


ETH zürich

Taekwang Jang

ETH zürich

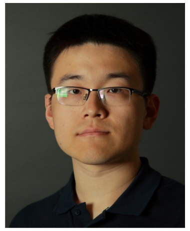
Tobi Delbruck

Universität Zürich[UZH]

Shih-Chii Liu

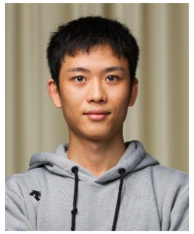
KAIST

Hoi-Jun Yoo

TU Delft

Chang Gao

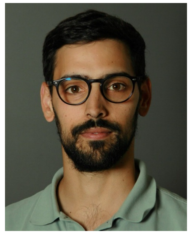
Universiteit Leiden

Qinyu Chen

ETH zürich

Sheng Zhou

csem

Xi Chen

ETH zürich

Rui Graça

ETH zürich

Ilya Kiselev

Berkeley University of California

Surin Gweon

KAIST

Ji-Hoon Kim

KAIST

Sangyeob Kim


# Thank you!

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